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ATX
Ver: 1.1

Intel -Shark Bay platform Z97

CPU:

Marswell Reflash LGA1150

System Chipset:

Z97

Onboard Chip:

HD Audio Codec:ALC1150

LAN-Killer E2205

SIO:Fintek NTC6792D

Flash ROM: SPI 64 MB

Main Memory:

*DDRIII (800/1066/1333MHz) * 4 (Dual Channel)*

ACPI:

UPI

PWM:

VRD12.5 -UP1649-8Phase

Expansion Slots:

*PCI Express (X16) Slot *3*

*PCI Express (X1) Slot * 4*

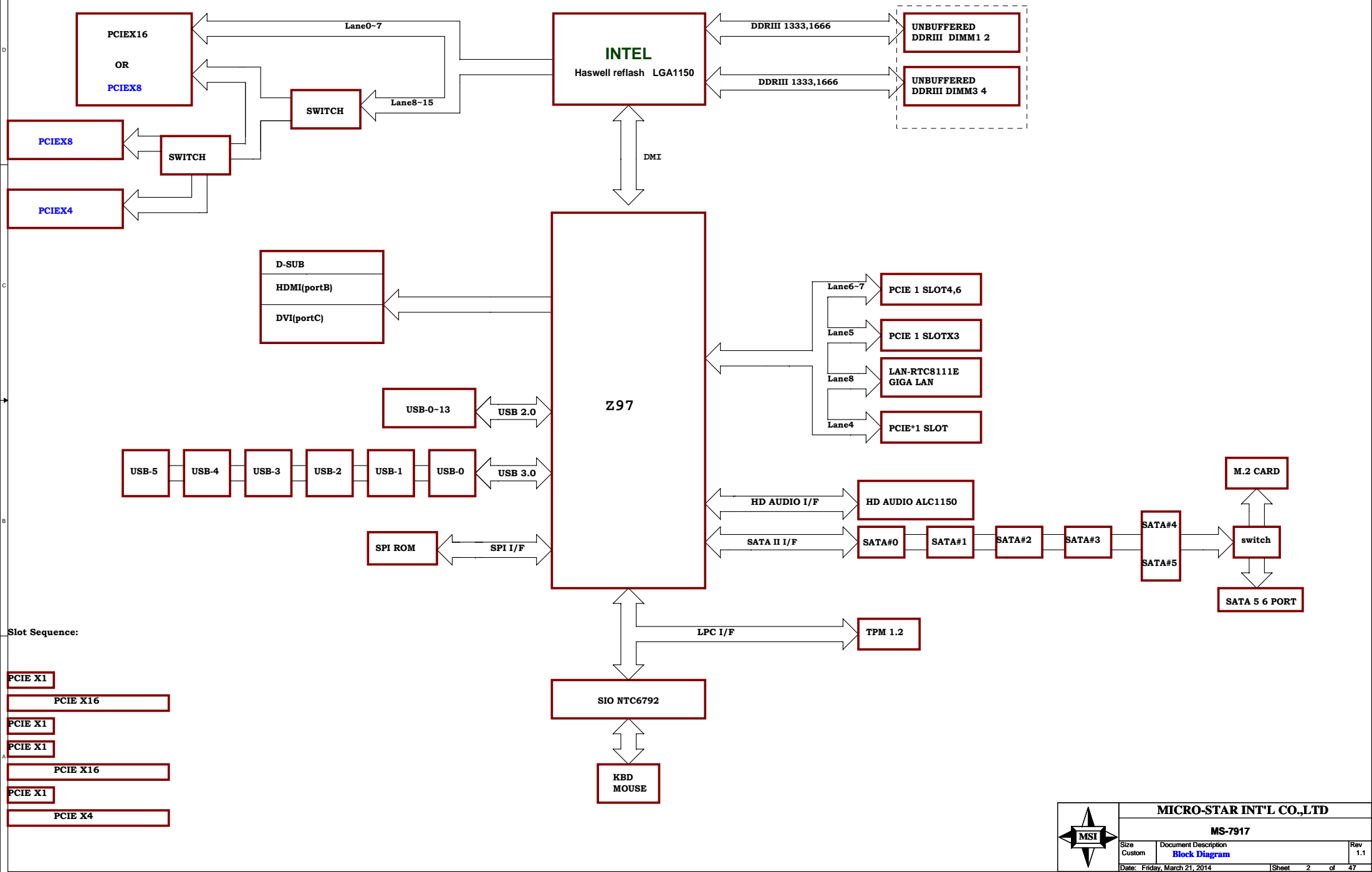
Other:

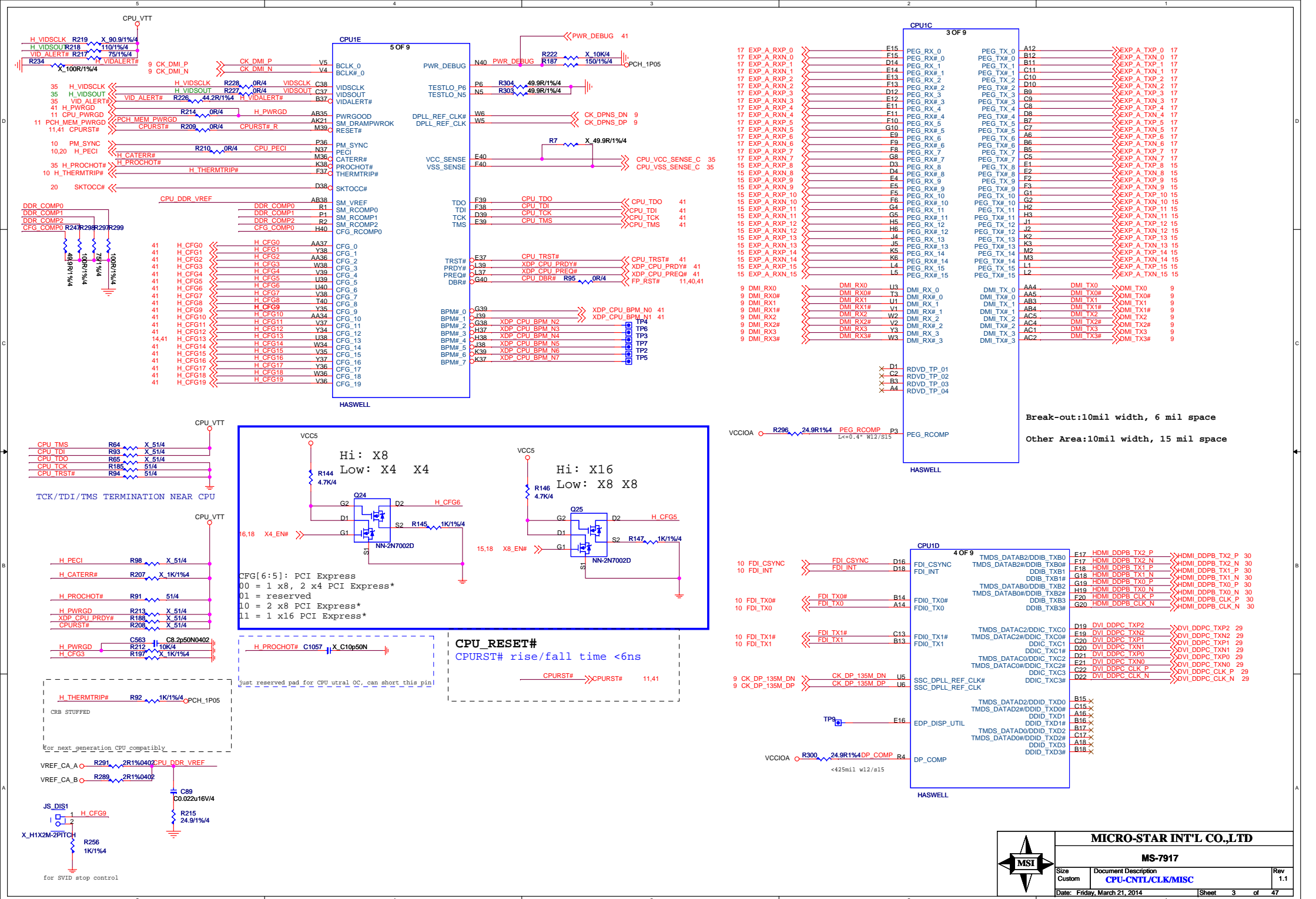
*SATA3.0 x6 (PCH)
REAR USB2.0 *4
FRONT USB2.0 *4
REAL USB3.0 *4
FRONT USB3.0 *2*

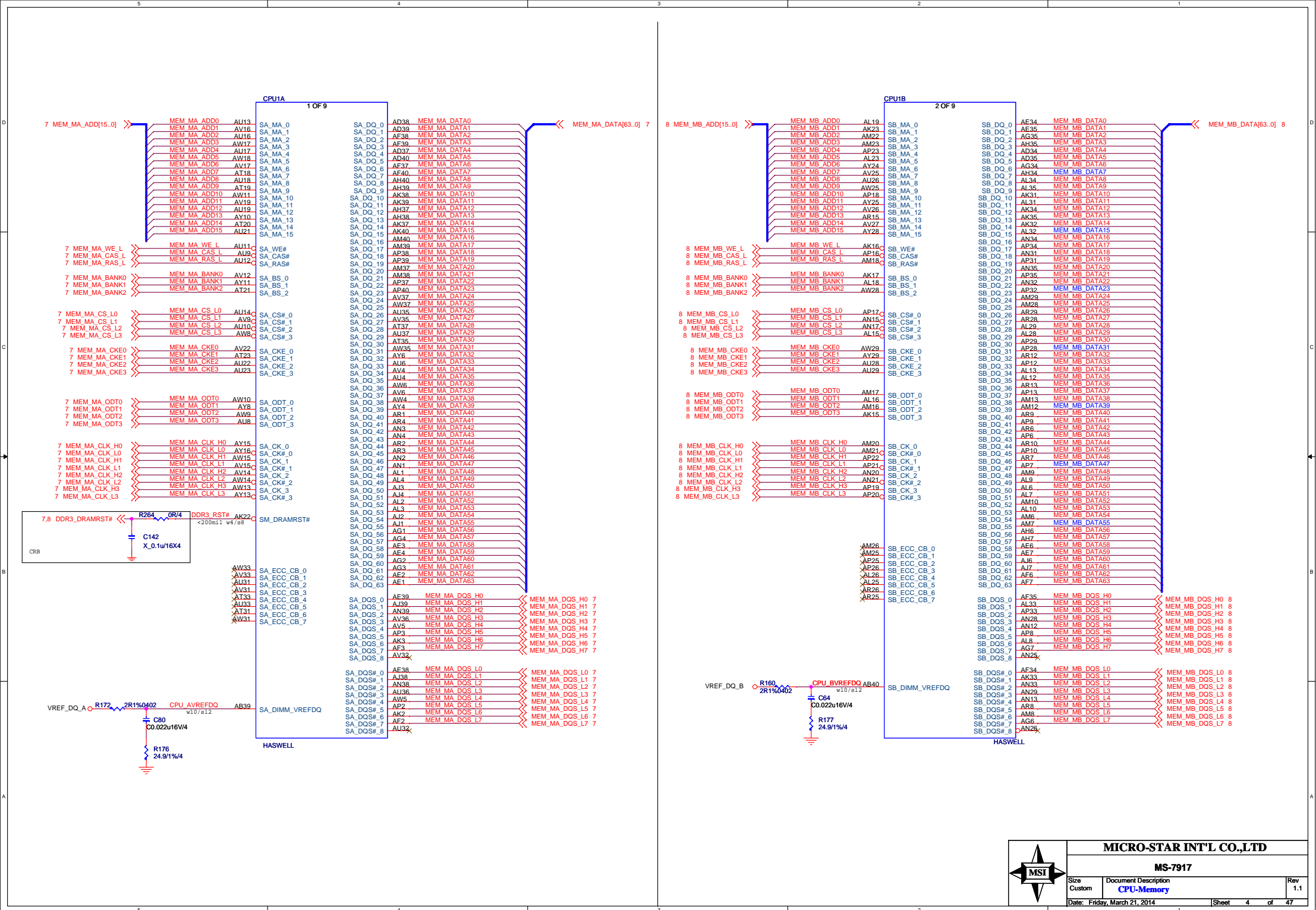


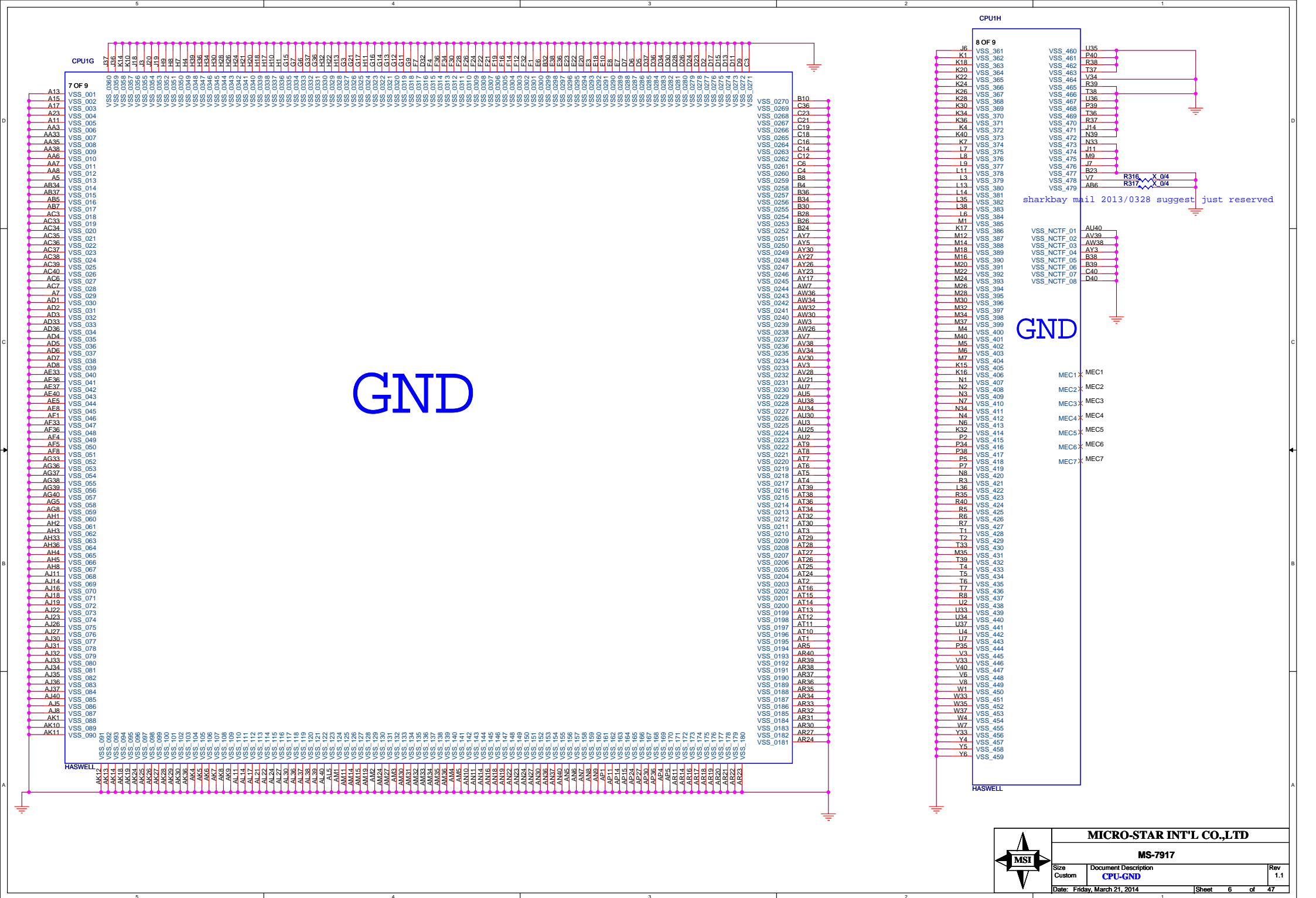
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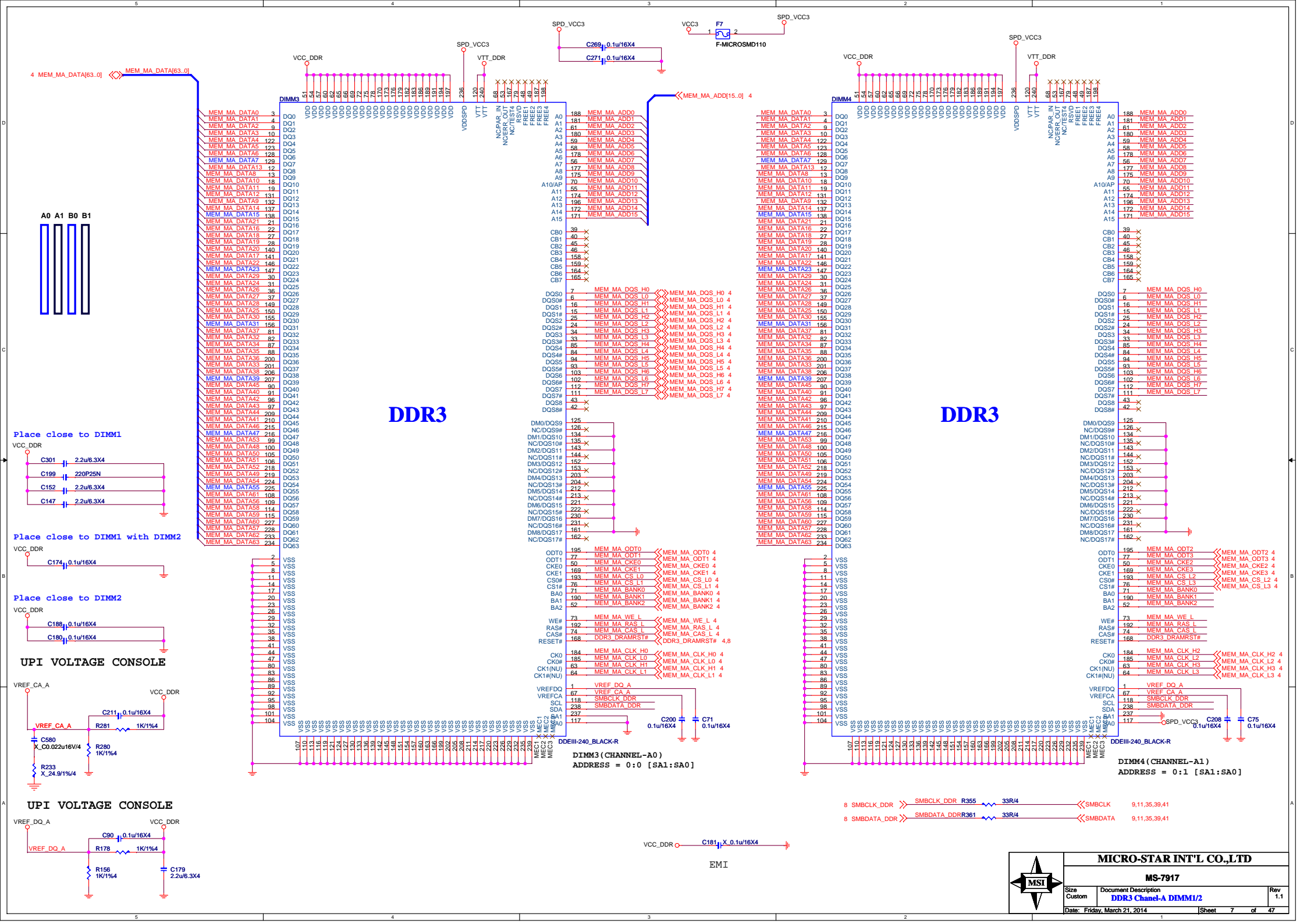
MS-7917 Block Diagram



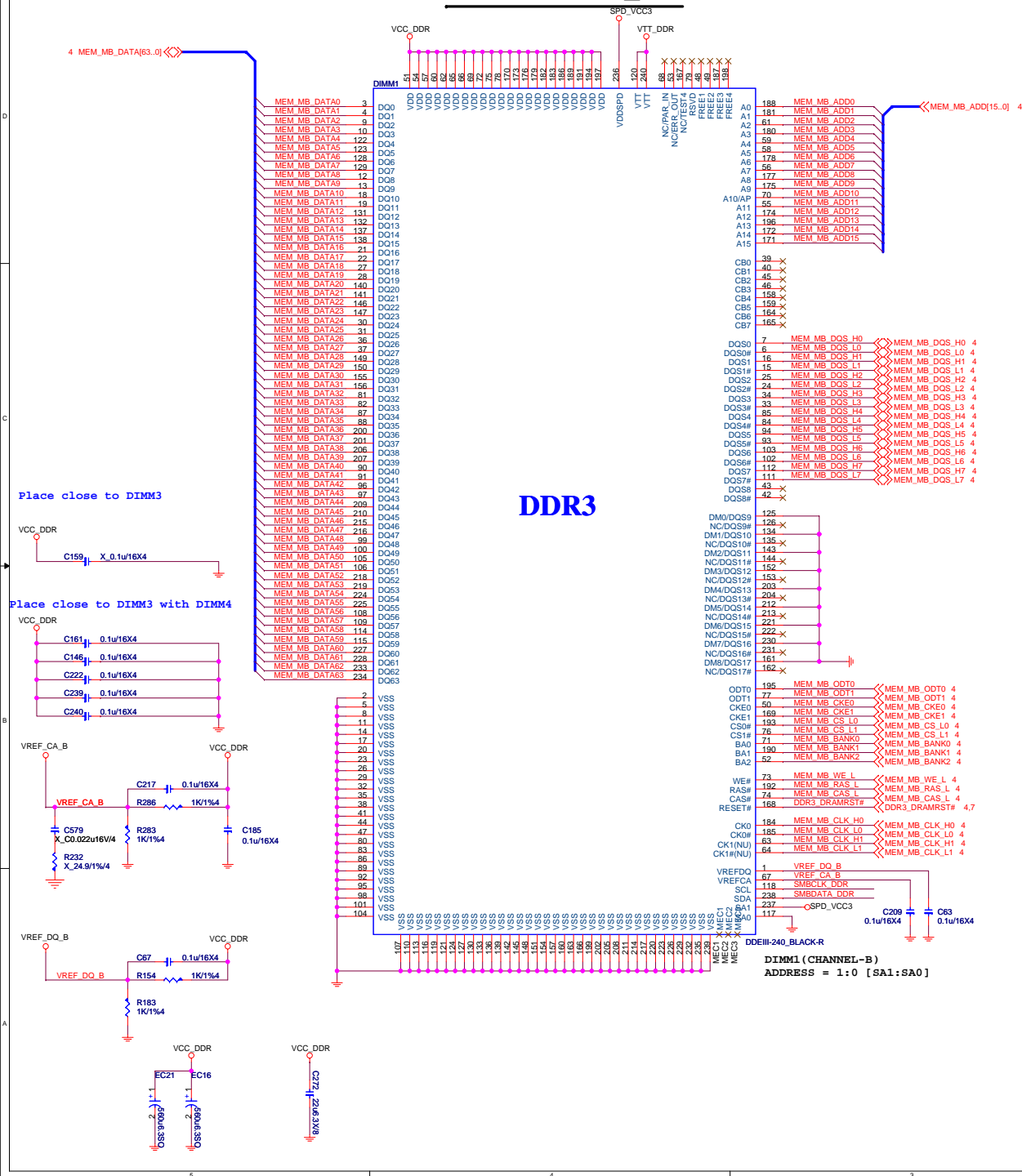




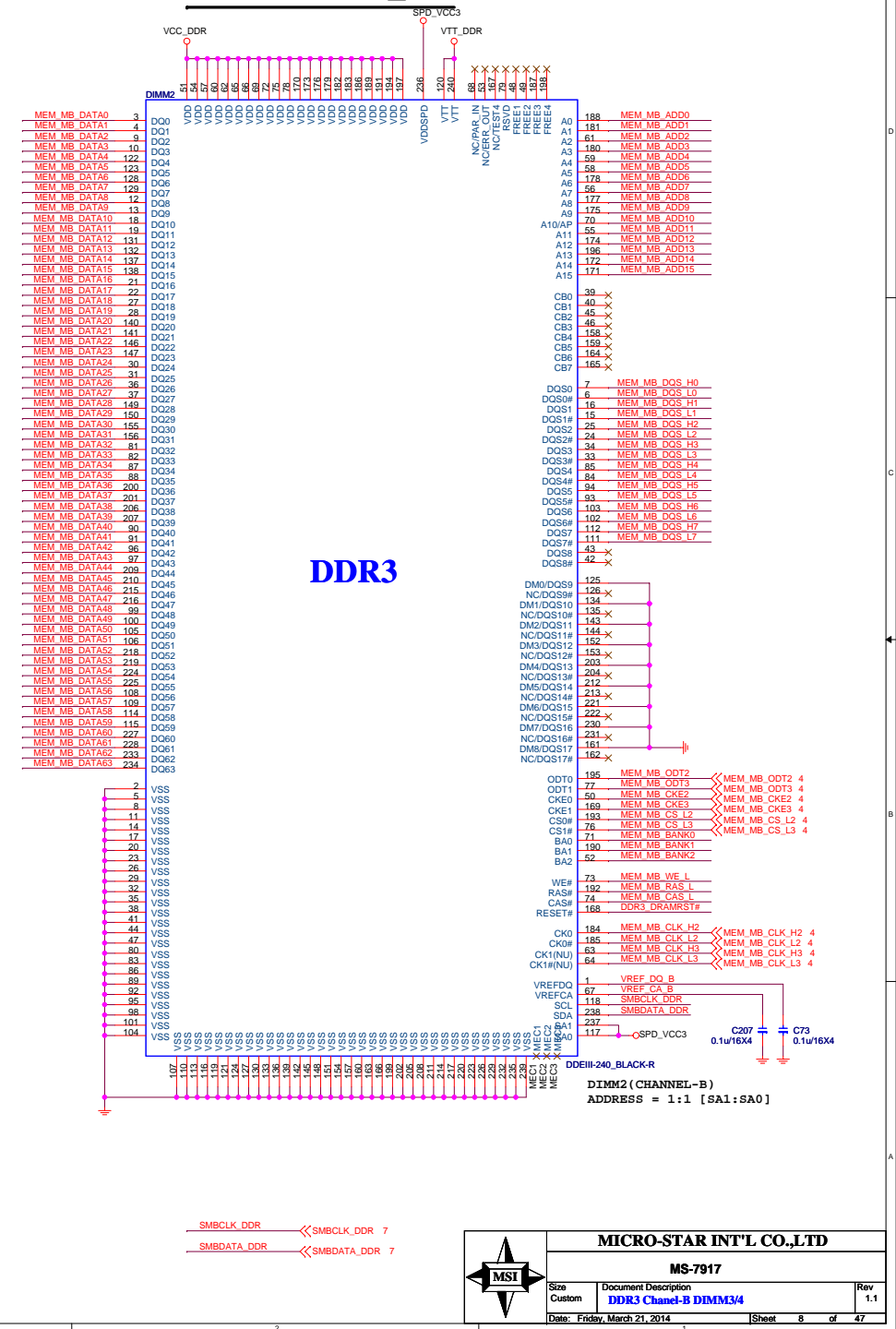


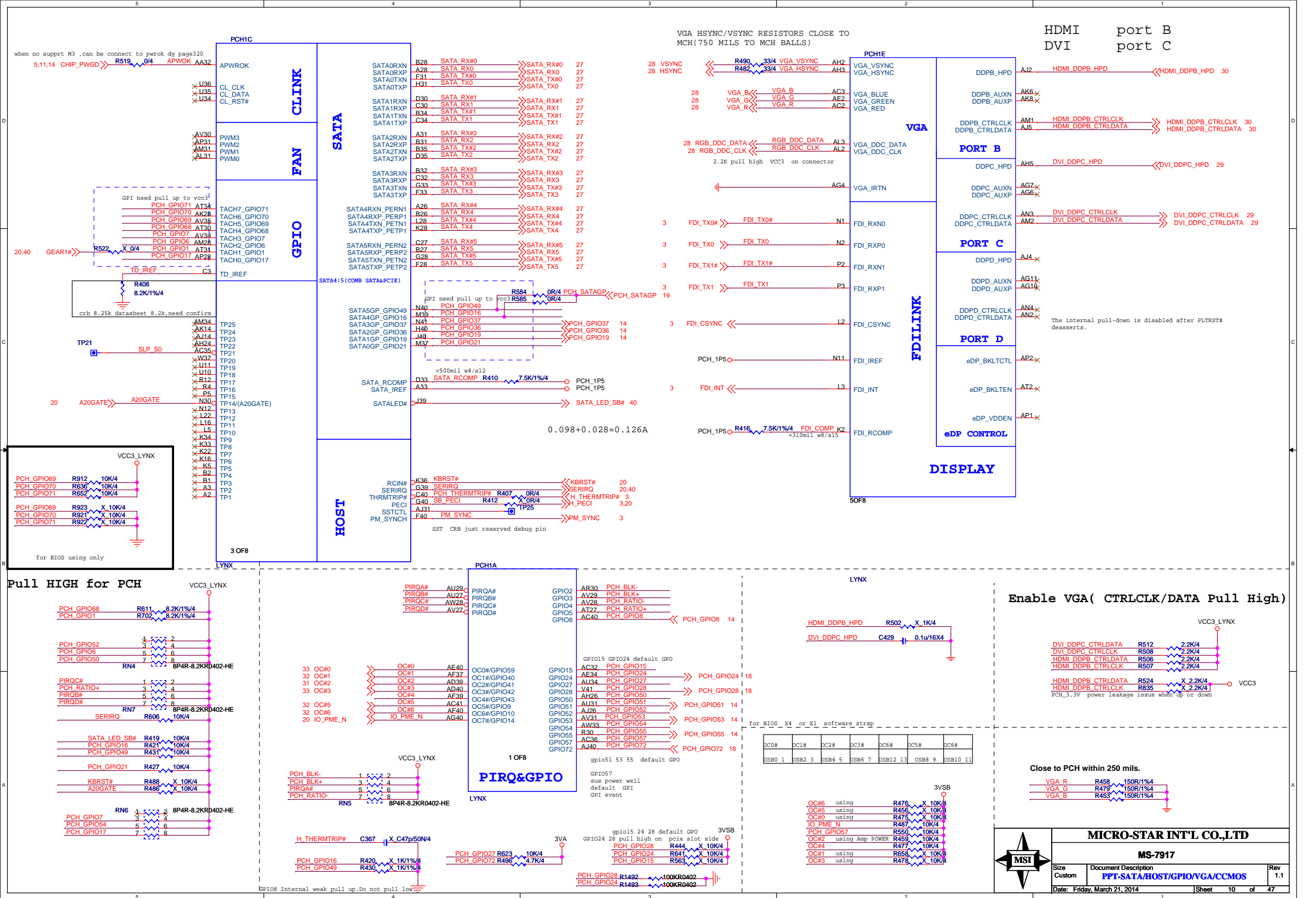


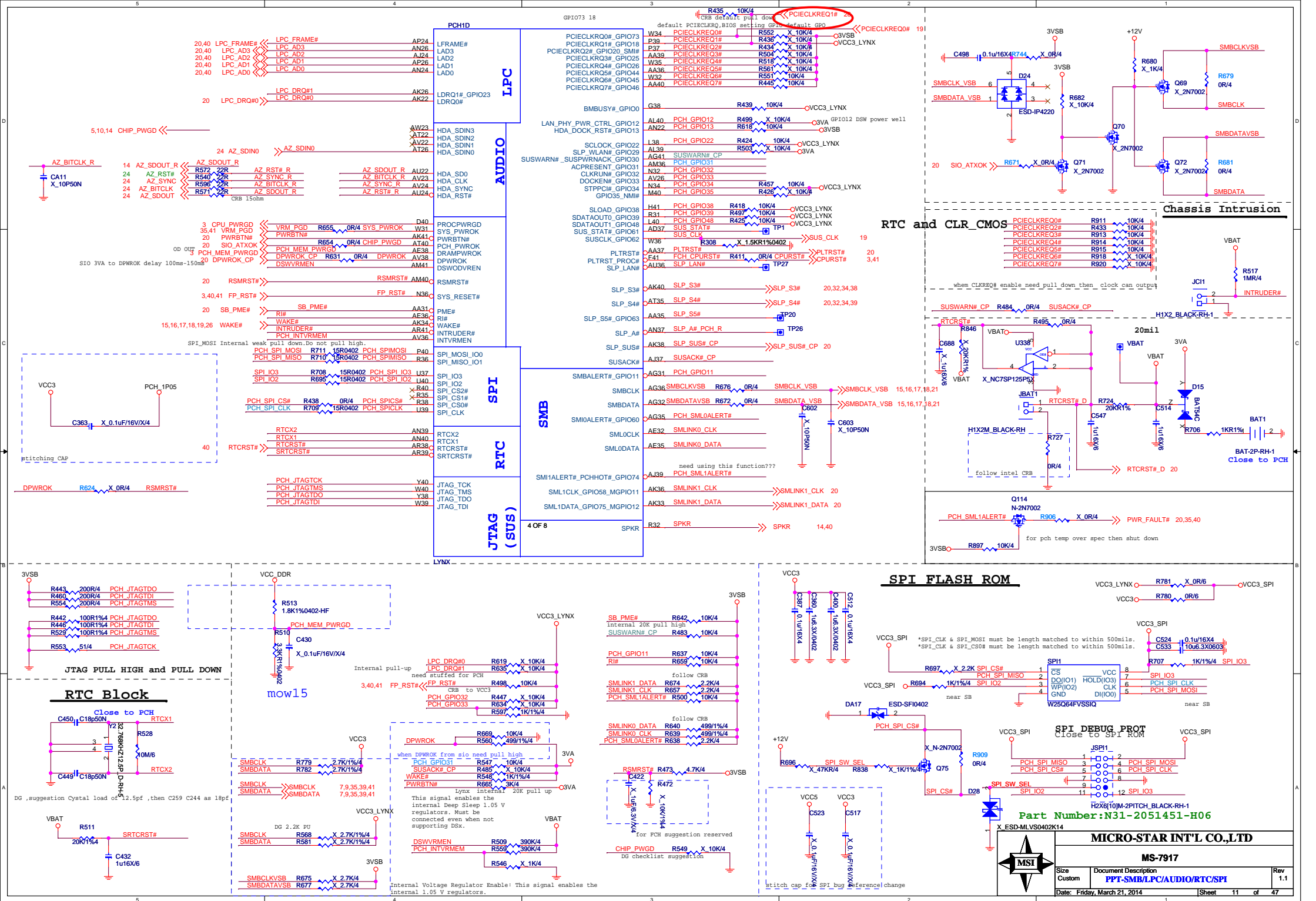
DDRIII DIMM_B0

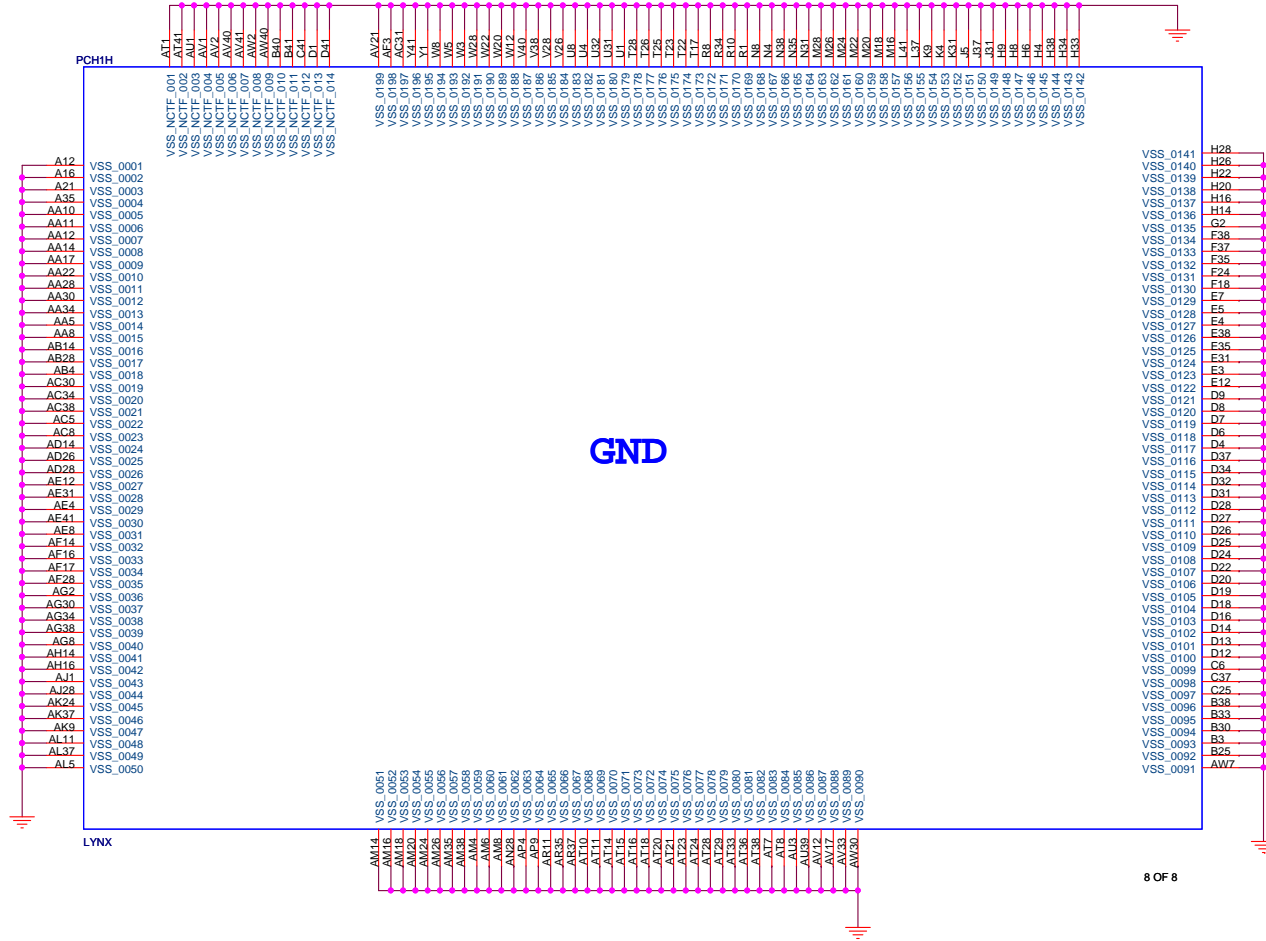


DDRIII DIMM_B1







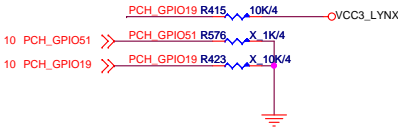


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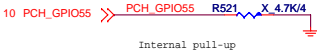
PCH Straps



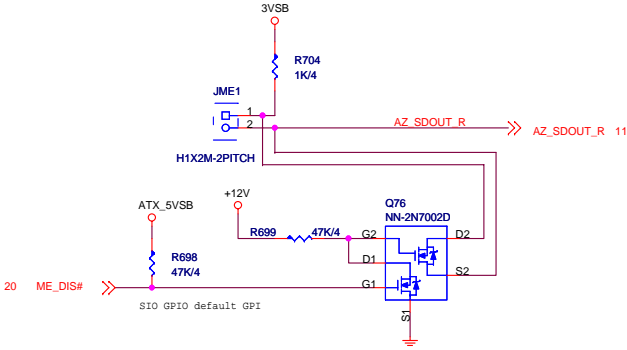
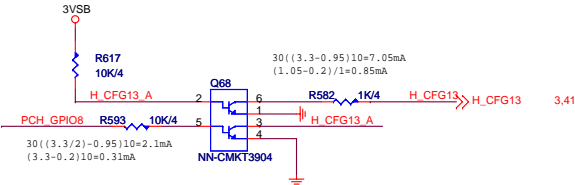
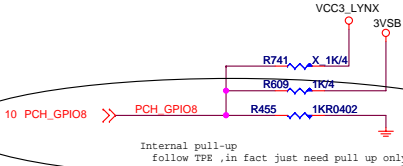
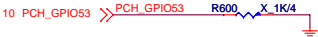
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1



Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pull-down
resistor.



Connect to ground with 1k Ohm pull-down
resistor.



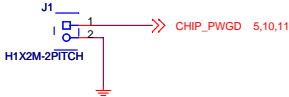
Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up
resistor through a jumper.




Internal weak pull down. Do not pull high.



GPIO37 Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.





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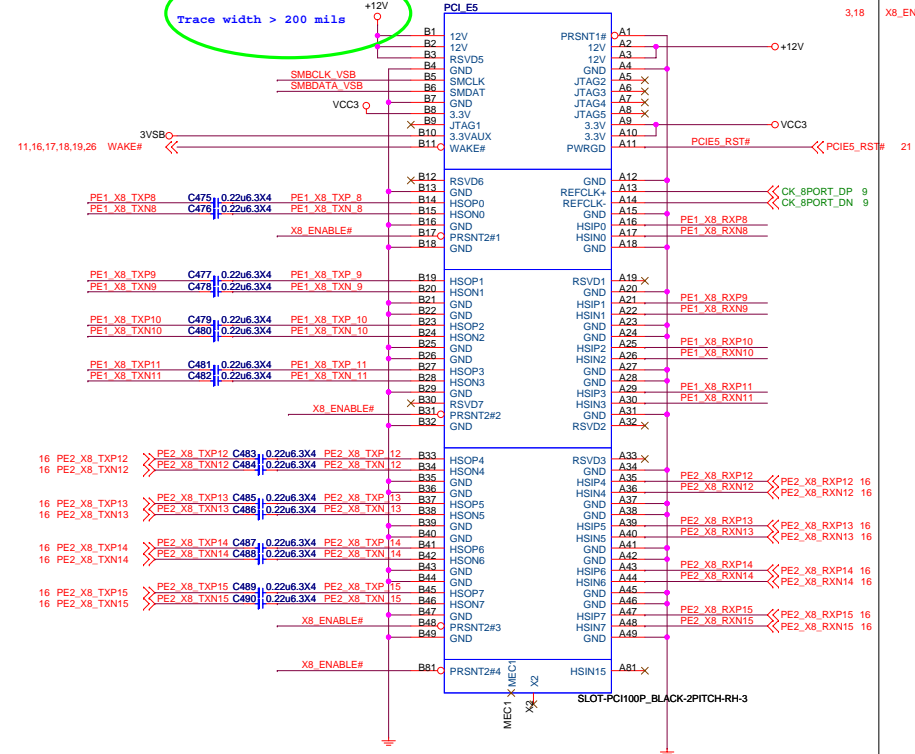
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PCI Express X8 Slot (Share with PCI_E x16 Slots)

11,16,17,18,21 SMBCLK_VSB
11,16,17,18,21 SMBDATA_VSB

Trace width > 200 mils



3 EXP_A_RXN_9
3 EXP_A_RXP_9
3 EXP_A_TXN_9
3 EXP_A_TXP_9

3,18 X8_EN#

3 EXP_A_RXN_8
3 EXP_A_RXP_8
3 EXP_A_TXN_8
3 EXP_A_TXP_8

3 EXP_A_RXN_13
3 EXP_A_RXP_13
3 EXP_A_TXN_13
3 EXP_A_TXP_13

3 EXP_A_RXN_12
3 EXP_A_RXP_12
3 EXP_A_TXN_12
3 EXP_A_TXP_12

3 EXP_A_RXN_15
3 EXP_A_RXP_15
3 EXP_A_TXN_15
3 EXP_A_TXP_15

3 EXP_A_RXN_14
3 EXP_A_RXP_14
3 EXP_A_TXN_14
3 EXP_A_TXP_14

3 EXP_A_RXN_11
3 EXP_A_RXP_11
3 EXP_A_TXN_11
3 EXP_A_TXP_11

3 EXP_A_RXN_10
3 EXP_A_RXP_10
3 EXP_A_TXN_10
3 EXP_A_TXP_10

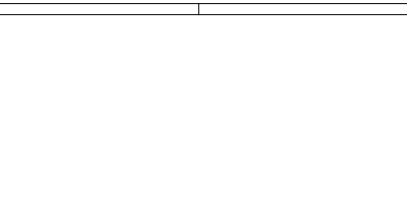
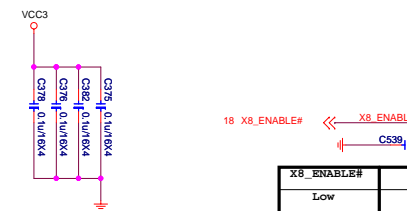
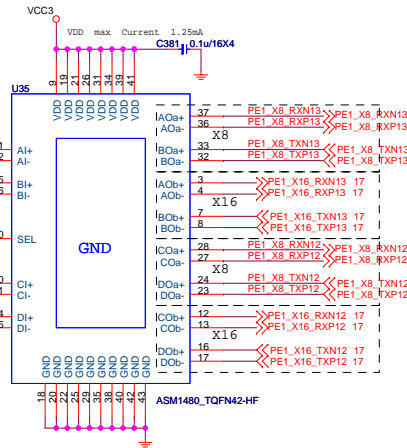
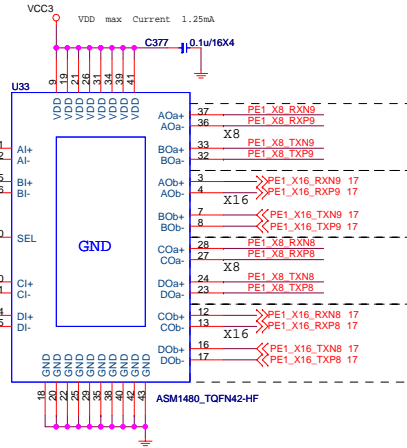
3 EXP_A_RXN_7
3 EXP_A_RXP_7
3 EXP_A_TXN_7
3 EXP_A_TXP_7

3 EXP_A_RXN_6
3 EXP_A_RXP_6
3 EXP_A_TXN_6
3 EXP_A_TXP_6

3 EXP_A_RXN_5
3 EXP_A_RXP_5
3 EXP_A_TXN_5
3 EXP_A_TXP_5

3 EXP_A_RXN_4
3 EXP_A_RXP_4
3 EXP_A_TXN_4
3 EXP_A_TXP_4

3 EXP_A_RXN_3
3 EXP_A_RXP_3
3 EXP_A_TXN_3
3 EXP_A_TXP_3



3 EXP_A_RXN_11
3 EXP_A_RXP_11
3 EXP_A_TXN_11
3 EXP_A_TXP_11

3,18 X8_EN#

3 EXP_A_RXN_10
3 EXP_A_RXP_10
3 EXP_A_TXN_10
3 EXP_A_TXP_10

3 EXP_A_RXN_15
3 EXP_A_RXP_15
3 EXP_A_TXN_15
3 EXP_A_TXP_15

3 EXP_A_RXN_12
3 EXP_A_RXP_12
3 EXP_A_TXN_12
3 EXP_A_TXP_12

3 EXP_A_RXN_14
3 EXP_A_RXP_14
3 EXP_A_TXN_14
3 EXP_A_TXP_14

3 EXP_A_RXN_11
3 EXP_A_RXP_11
3 EXP_A_TXN_11
3 EXP_A_TXP_11

3 EXP_A_RXN_10
3 EXP_A_RXP_10
3 EXP_A_TXN_10
3 EXP_A_TXP_10

3 EXP_A_RXN_7
3 EXP_A_RXP_7
3 EXP_A_TXN_7
3 EXP_A_TXP_7

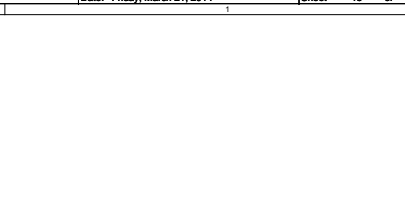
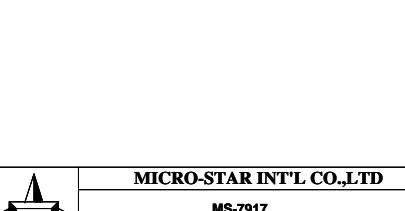
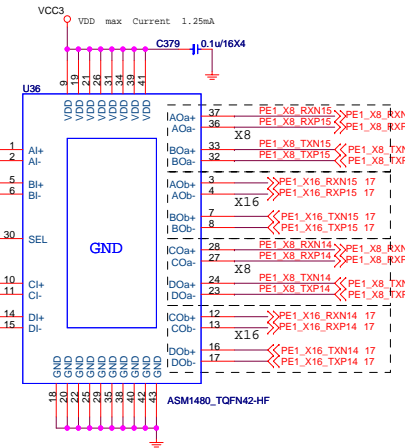
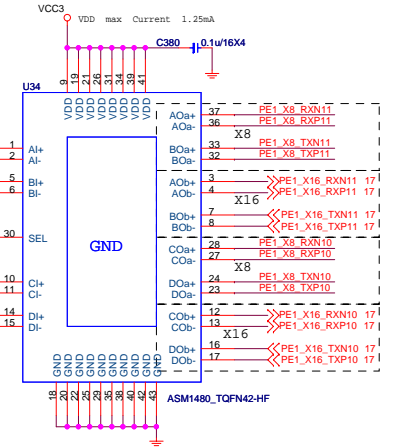
3 EXP_A_RXN_6
3 EXP_A_RXP_6
3 EXP_A_TXN_6
3 EXP_A_TXP_6

3 EXP_A_RXN_5
3 EXP_A_RXP_5
3 EXP_A_TXN_5
3 EXP_A_TXP_5

3 EXP_A_RXN_4
3 EXP_A_RXP_4
3 EXP_A_TXN_4
3 EXP_A_TXP_4

3 EXP_A_RXN_3
3 EXP_A_RXP_3
3 EXP_A_TXN_3
3 EXP_A_TXP_3

3 EXP_A_RXN_2
3 EXP_A_RXP_2
3 EXP_A_TXN_2
3 EXP_A_TXP_2



X8_ENABLE#	PCI-E Slot 1/2
Low	X8 / X8
H1	X16

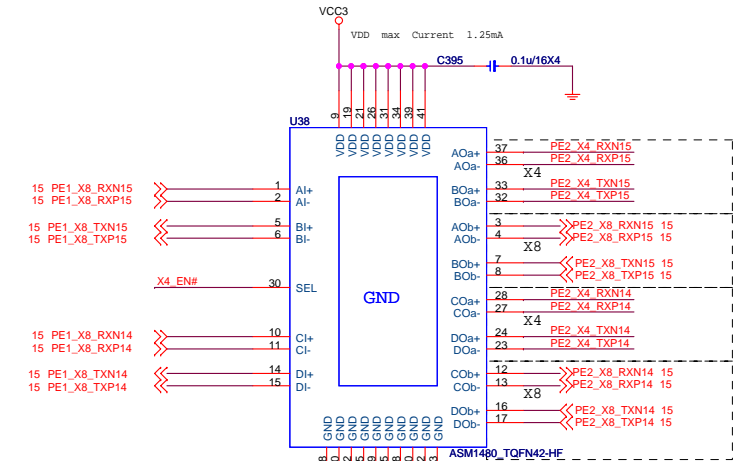
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support max speed GEN2
```

+12V



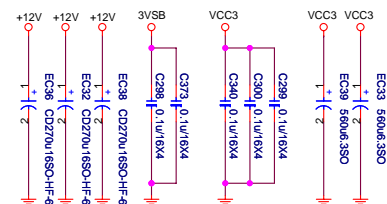
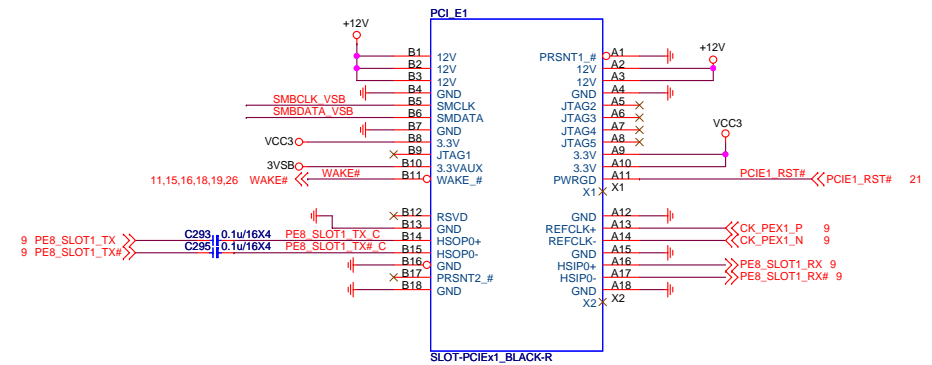
WITHIN 500m11

18 X4_ENABLE#MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description PCIE(X4) & PCIE(X1) slots	Rev 1.1
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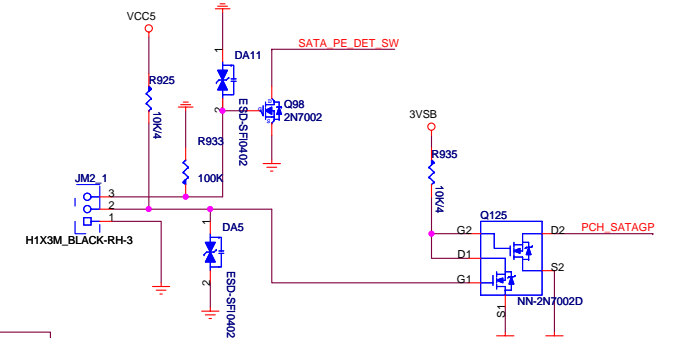
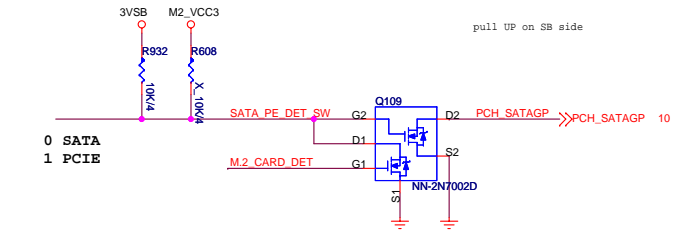
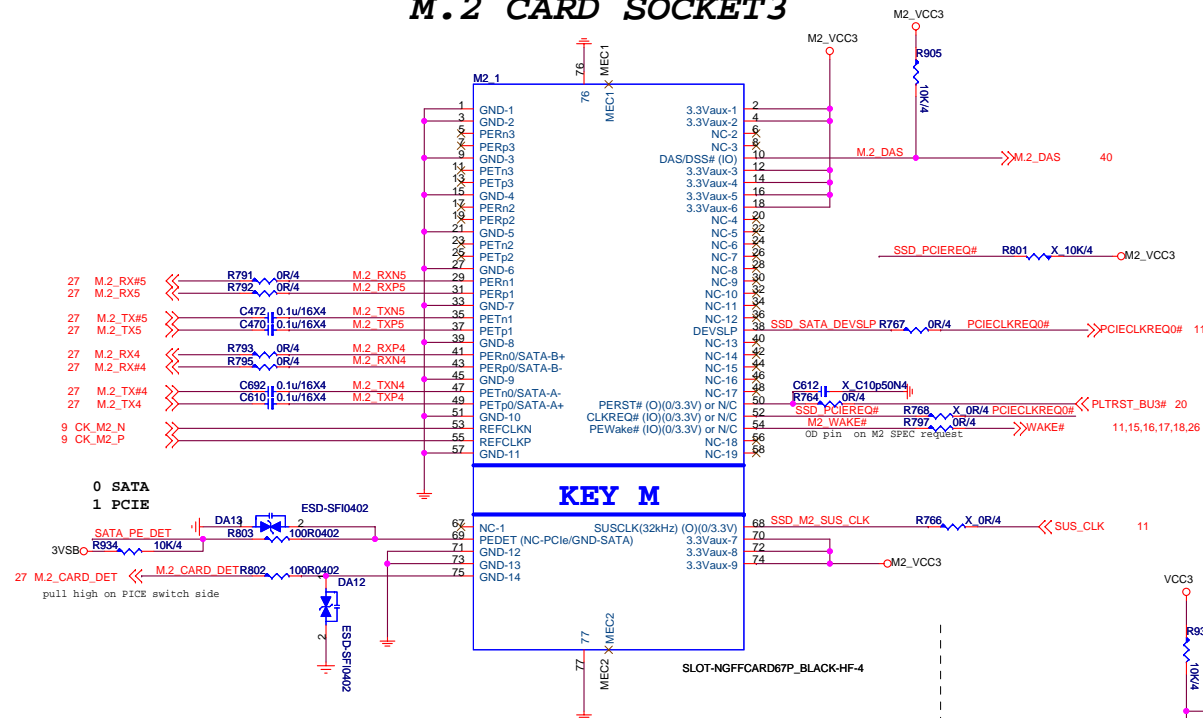
MICRO-STAR INT'L CO.,LTD			
MS-7917			
Size Custom	Document Description PCIE1(X1) & PCIE2(X16) Slots		Rev 1.1
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Size Custom	Document Description PCIE3(X1) & PCIE4(X1) Slots	Rev 1.1
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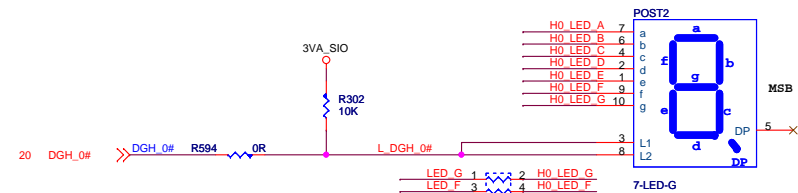
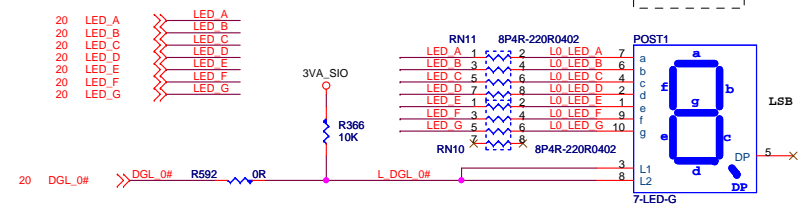
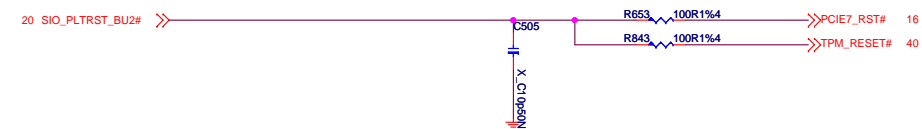
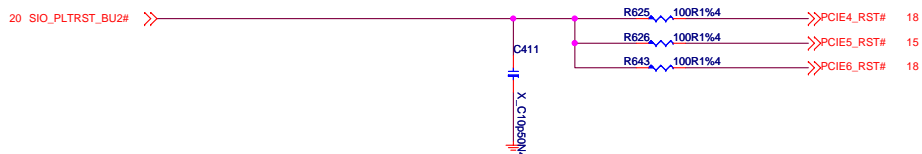
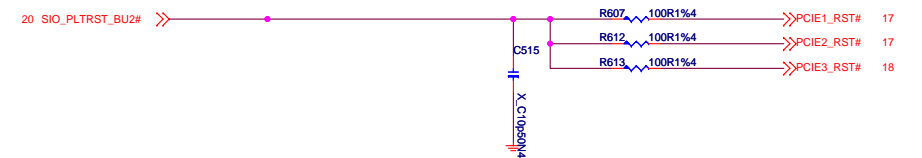
M.2 CARD SOCKET3



	SATA CARD	PCIE CARD	NA	NO CARD
SATA_PE_DET	0	1	0	1
M2_CARD_DET	0	0	1	1
SATA4/5GP	1	0	1	1

SATA4GP/SATA5GP
for chipset that main power, if pull up to VSB maybe will leakage power
If sampled value = 1, select SATA; if sampled value = 0, select PCIE

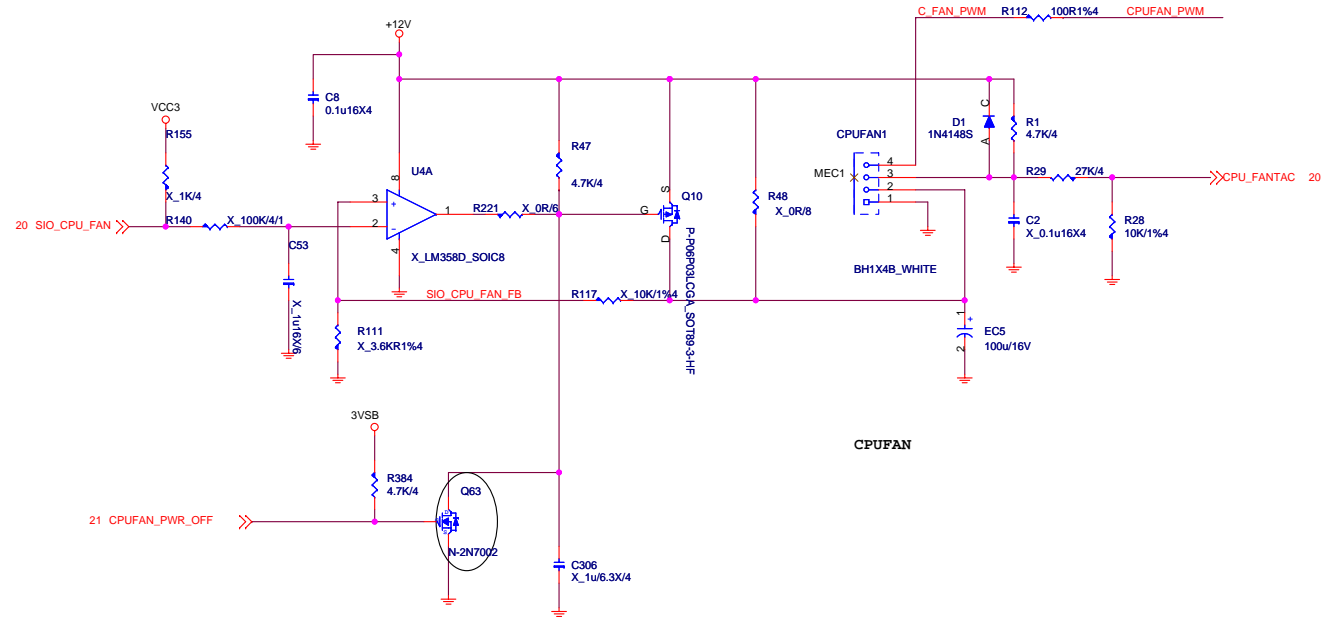
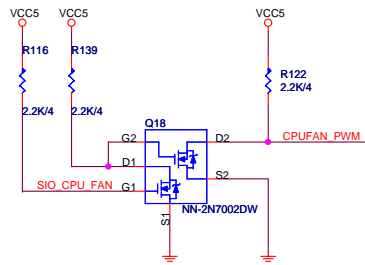
For EMI solution 2008-12-03



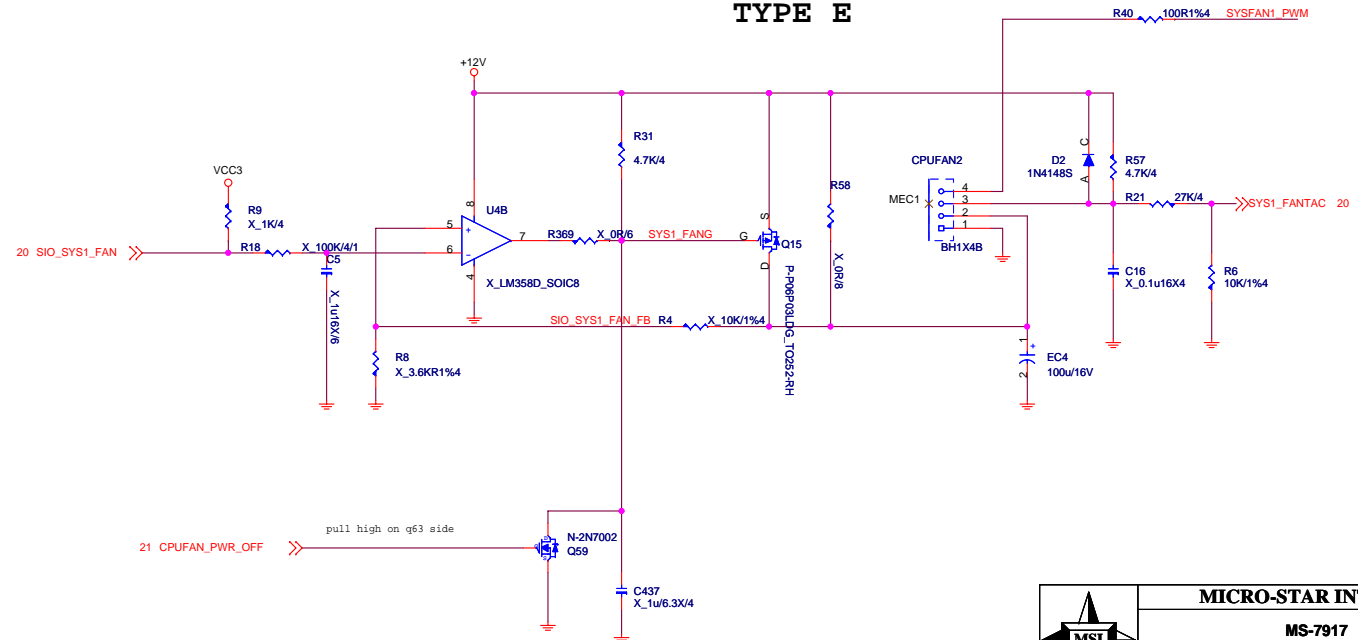
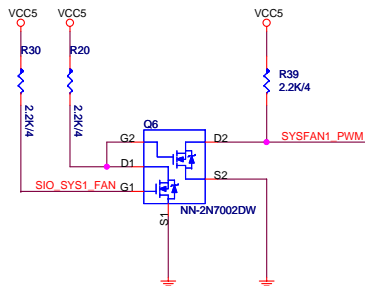
Size Custom	Document Description PS2 AND DEBUG LED	Rev 1.1
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FAN-COUNTROL CIRCUIT

TYPE E



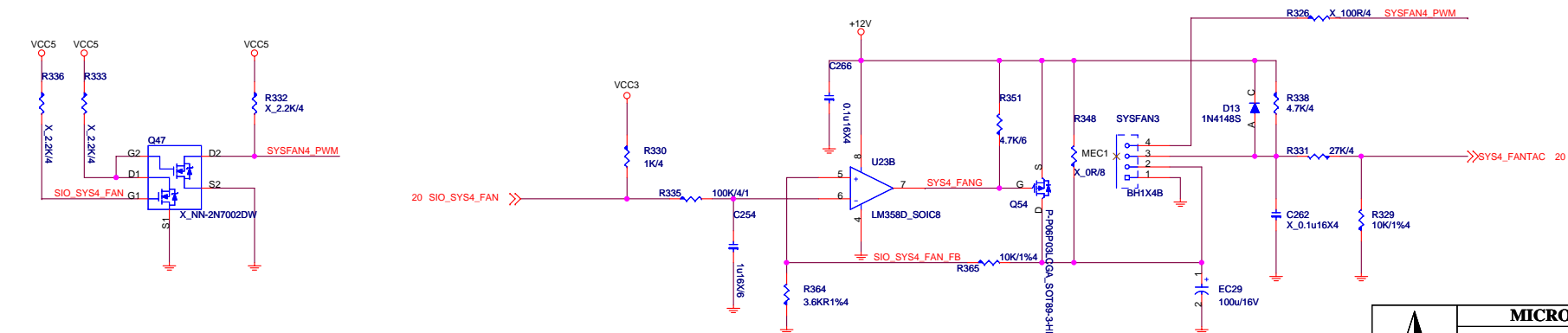
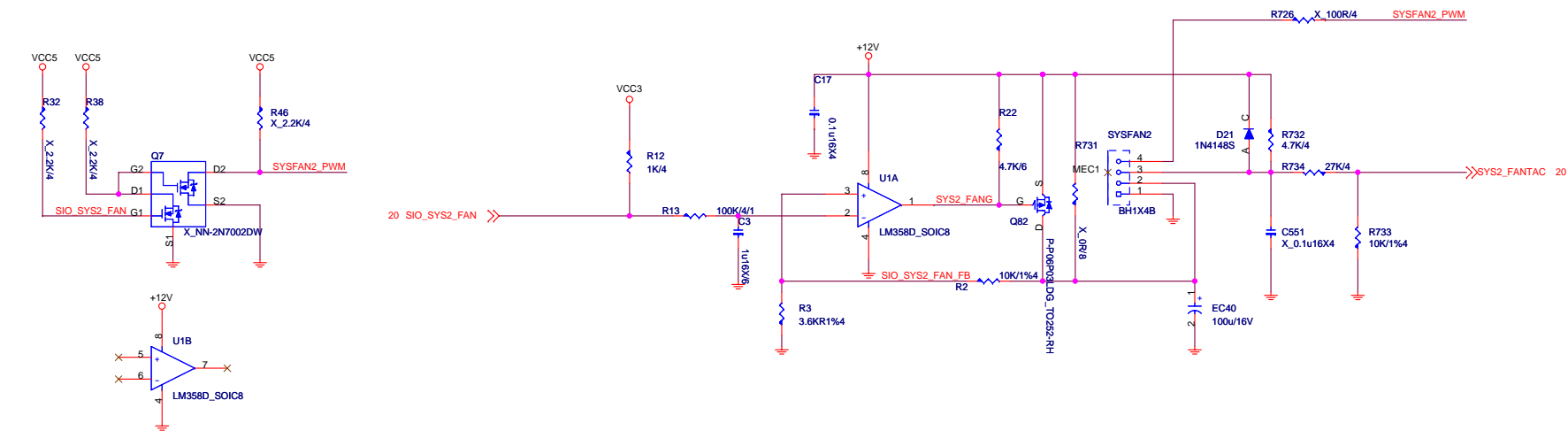
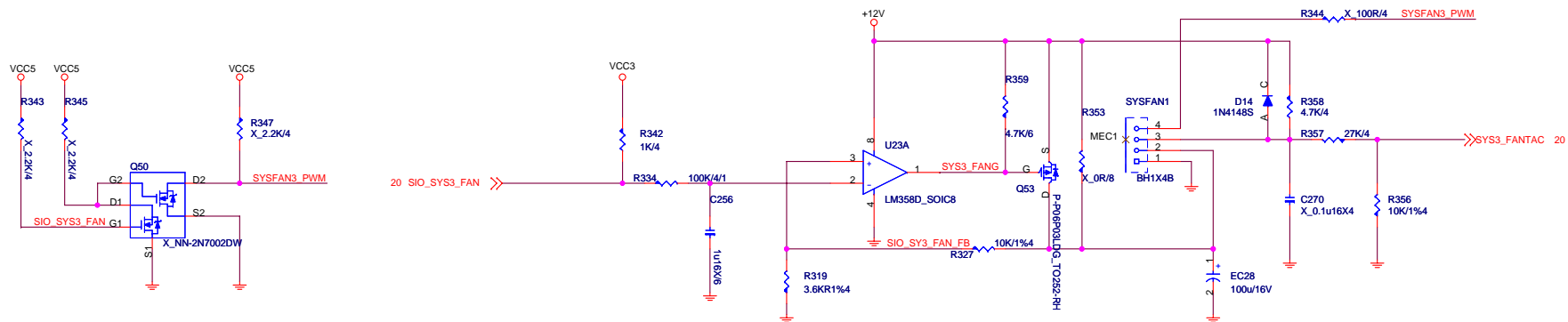
TYPE E

$$\begin{aligned}(1.05-0.9)/4.7 &= 0.03\text{mA} \\ (5-0.2)/20 &= 0.24\text{mA} \\ 30 \times 0.03 &> 0.24\end{aligned}$$


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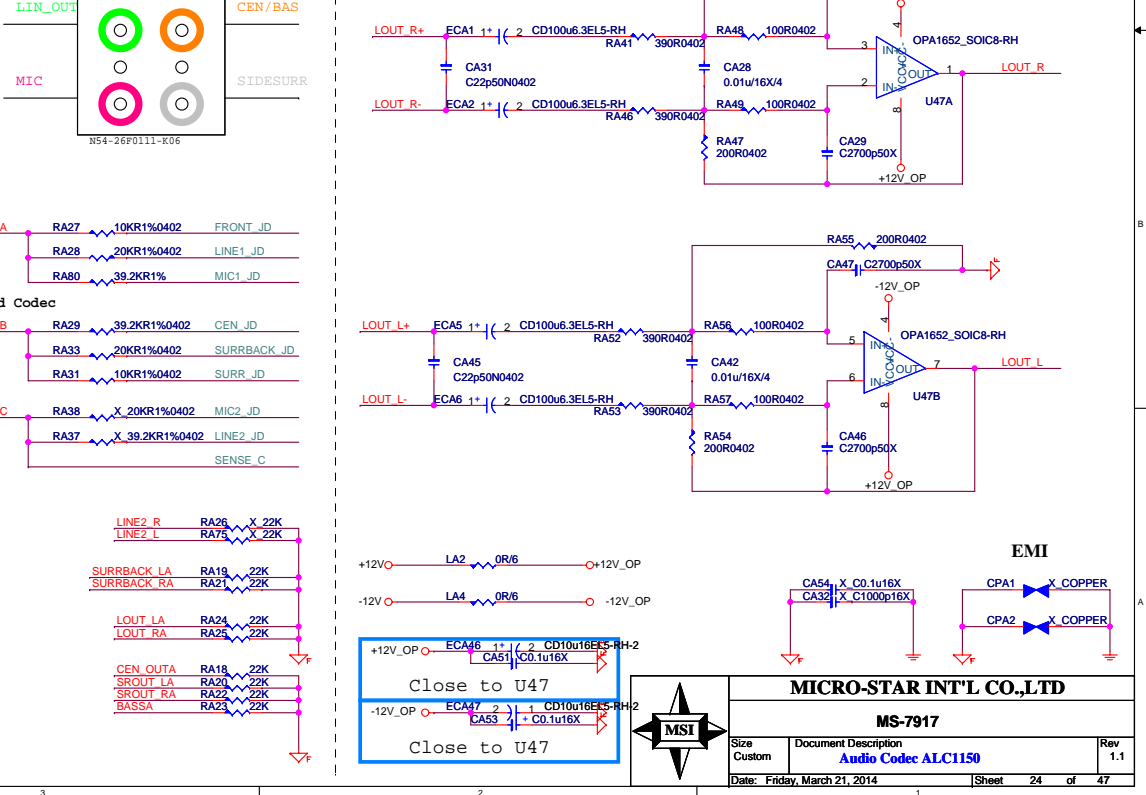
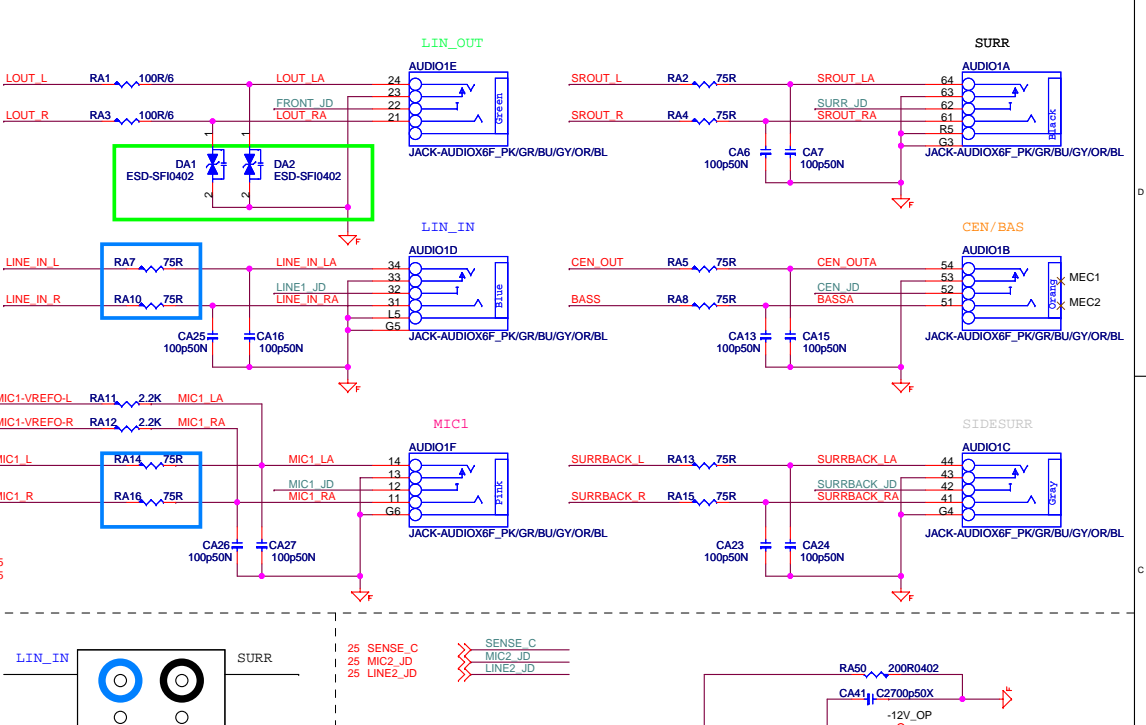
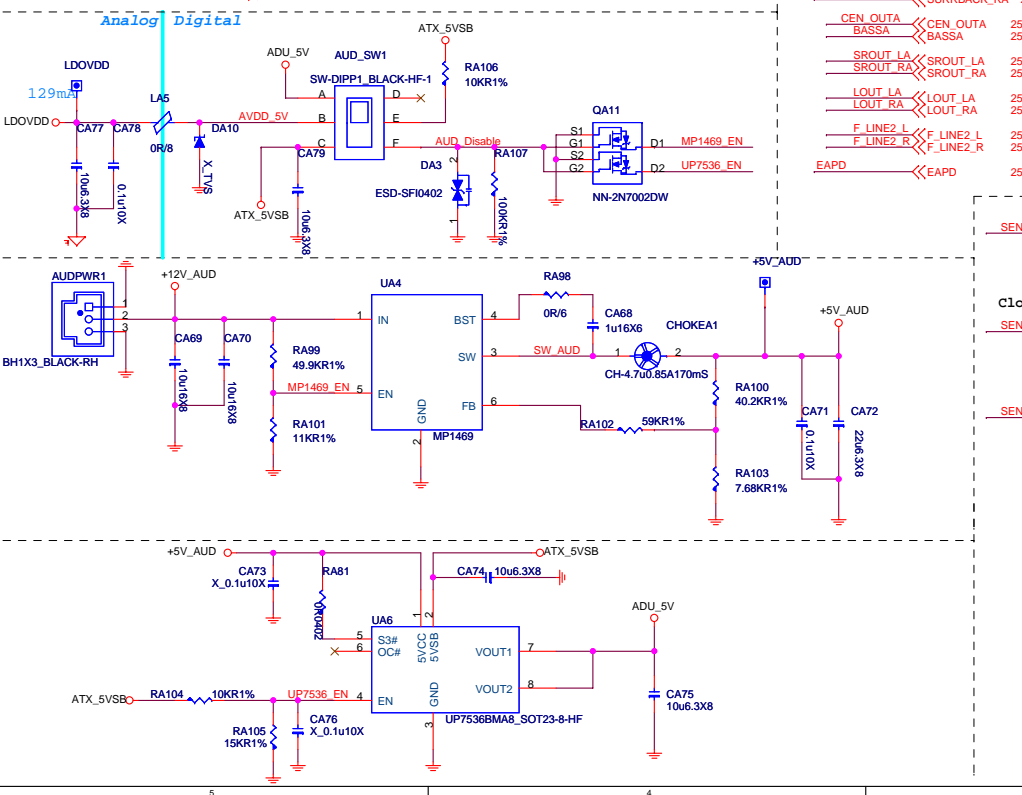
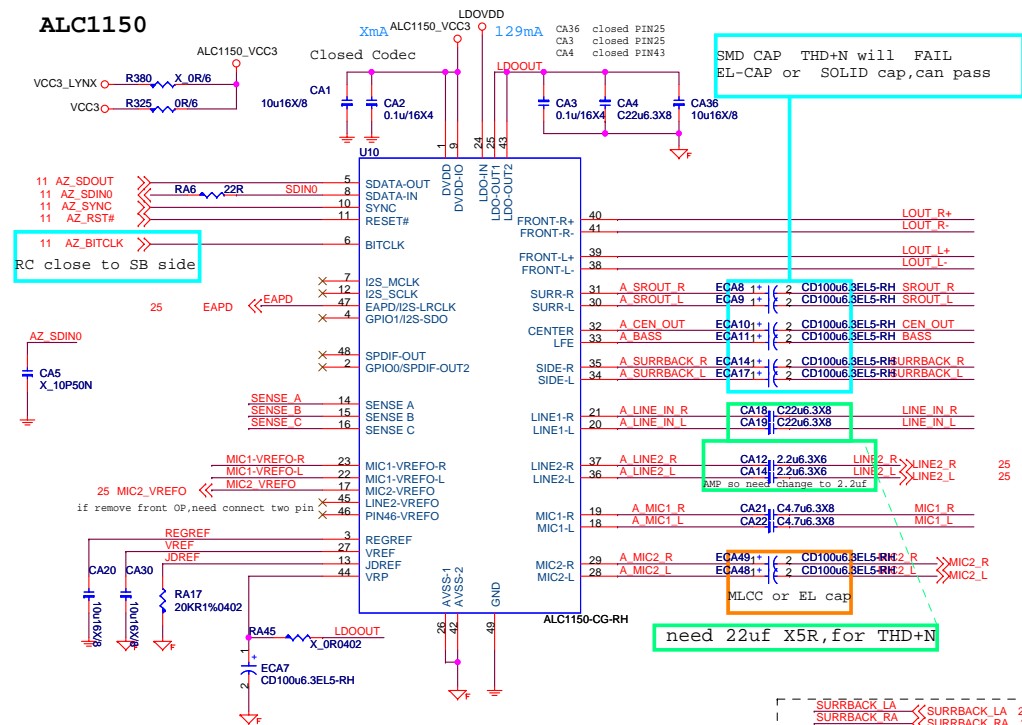


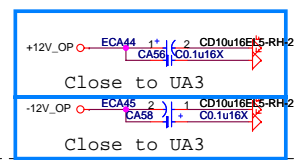
MICRO-STAR INT'L CO.,LTD

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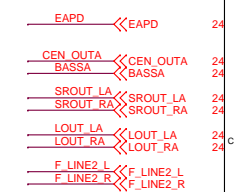
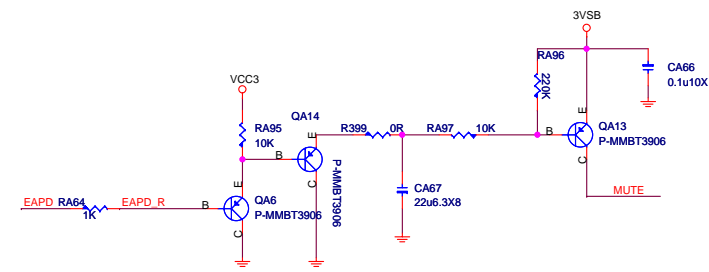
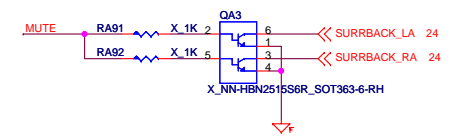
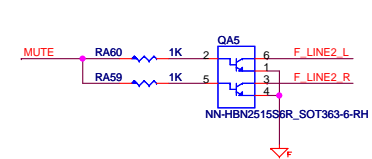
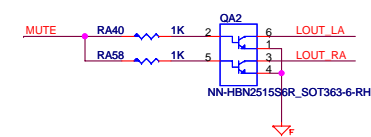
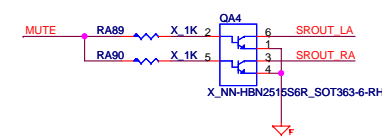
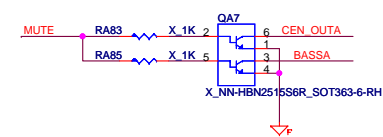
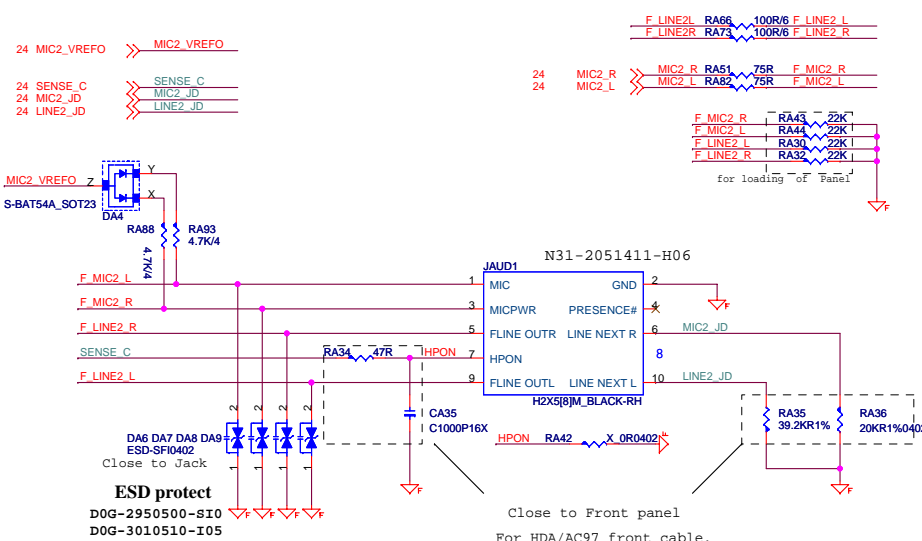
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ALC1150

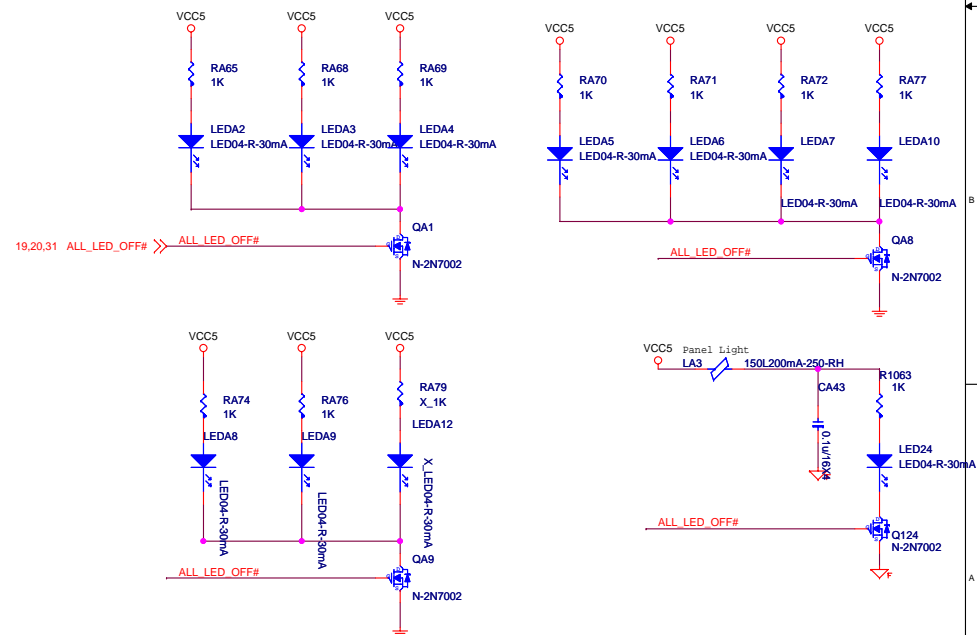




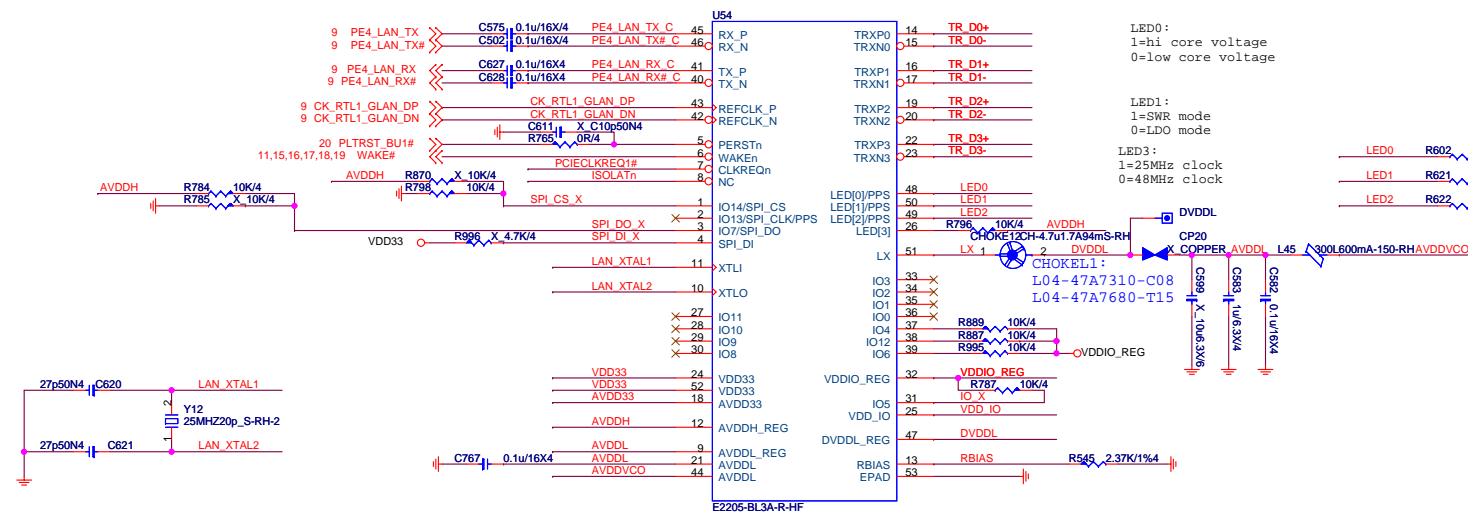
if remove front OP need add front line REF



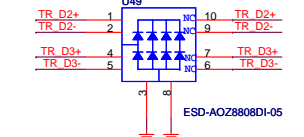
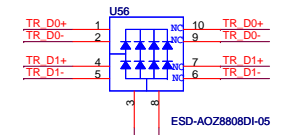
audio de-pop circuit



AUDIO MOAT NEED 40MIL



```
VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDD_IO power trace should be wider than 30mils;  
VDDIO_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.
```



D0G-05A050C-005
D0G-05A0300-I14
D0G-06A050C-A68

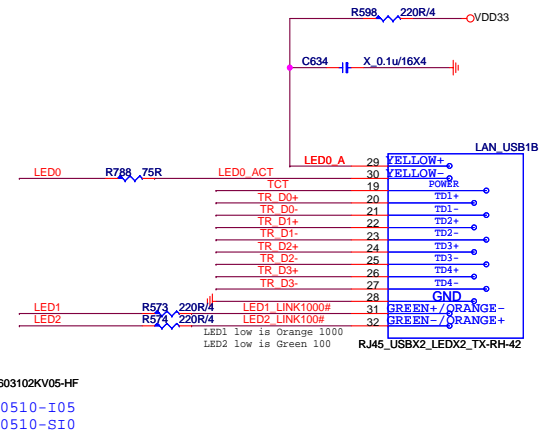
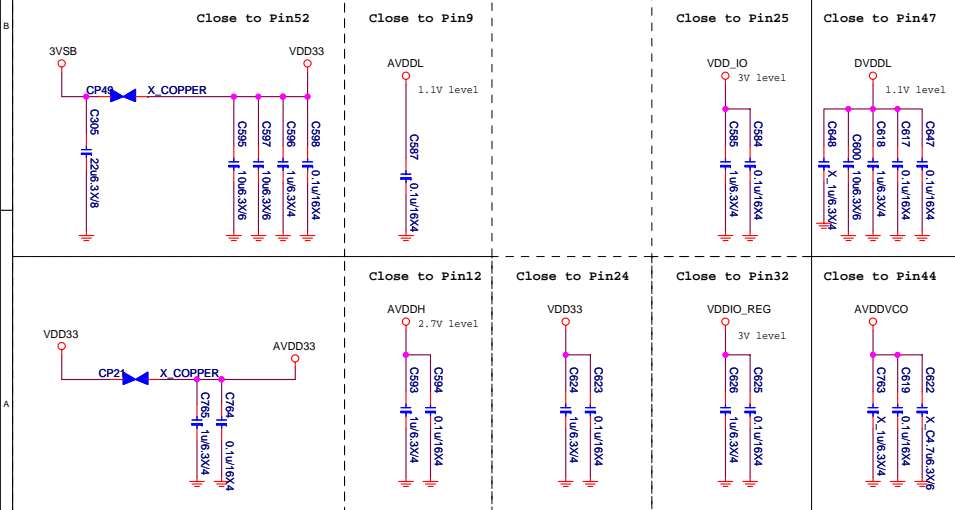
Remove pull-up R if R4 existence on motherboard
(or SB has internal pull-up R).



```

0:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRI013.

```



MICRO-STAR INT'L CO.,LTD

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	Size
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	Document Description LAN-E2205
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Rev	
1.1	

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The diagram shows the internal wiring of the SATA14PM_BLACK-RH-2 component. It features four input/output pairs on the left: SATA_TX0, SATA_TX#0, SATA_RX#0, and SATA_RX0. These are connected to a central block labeled SATA14PM_BLACK-RH-2. The block has pins for GND, S3HT+1, S3HT-1, S3HR+1, S3HR-1, X1, X2, MEC1, and MEC2. On the right, the block is connected to components C441, C446, C451, C455, C456, C458, ST Tx1, ST Tx#1, ST Rx#1, and ST Rx1. The connections are labeled with values like 0.01u/16X/4 and ST TX0, ST TX#0, ST RX0, ST RX#0. The diagram also shows ground connections for the TX0, TX#0, RX0, and RX#0 lines.

SATA3_4

Pin	Signal	Connector Label
1	GND	
2	S3HT+1 S3HT-2	SATA TX2
3	S3HT-1 S3HT+2	SATA TX#2
4	GND	
5	GND	
6	S3HR-1 S3HR-2	SATA RX#2
7	S3HR+1 S3HR+2	SATA RX2
8	GND	
9	ST TX3 C501	SATA TX3
10	ST TX#3 C503	SATA TX#3
11	GND	
12	ST RX#3 C506	SATA RX#3
13	ST RX3 C507	SATA RX3
14	GND	
15	X1	
16	X2	

SATA14PM_BLACK-RH-2

SATA5_6

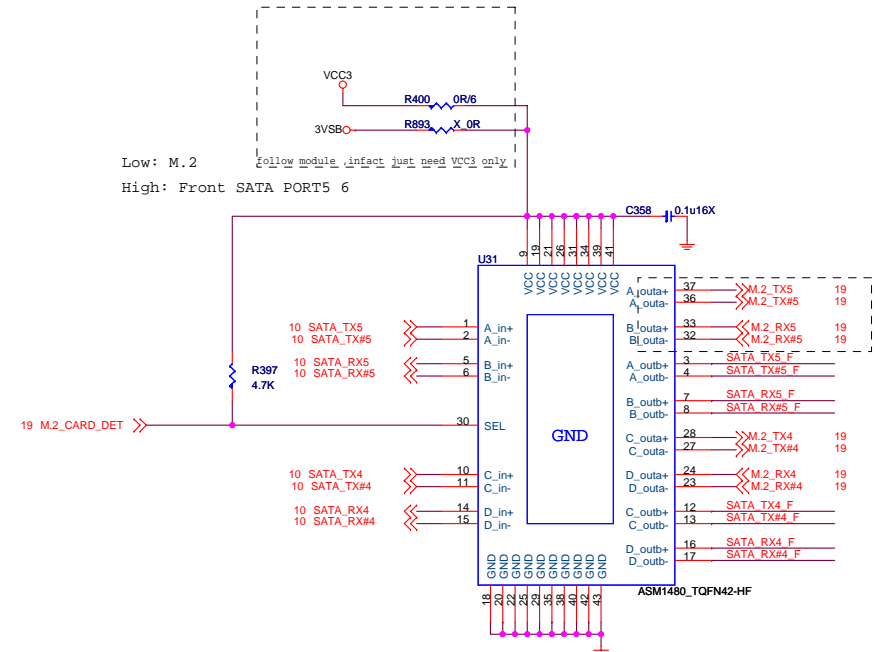
Signal	Connector Pin	Board Pin	Signal	Connector Pin	Board Pin
SATA TX4 F	C385	0.01u/16X4	ST TX4	8	C388
SATA TX#4 F	C386	0.01u/16X4	ST TX#4	9	C391
SATA RX#4 F	C404	0.01u/16X4	ST RX#5	11	C399
SATA RX4 F	C409	0.01u/16X4	ST RX5	12	C403

Other connections shown in the diagram include:

- Pin 1: GND
- Pin 2: S3HT-1 S3HT-2
- Pin 3: S3HT-1 S3HT-2
- Pin 4: GND
- Pin 5: S3HR-1 S3HR-2
- Pin 6: S3HR-1 S3HR-2
- Pin 7: GND
- Pin 8: GND
- Pin 9: S3HT-1 S3HT-2
- Pin 10: S3HT-1 S3HT-2
- Pin 11: S3HR-1 S3HR-2
- Pin 12: S3HR-1 S3HR-2
- Pin 13: GND
- Pin 14: GND

Ground connections: X1, X2, MEC1, MEC2, MEC3.

SATA14PM_BLACK-RH-2

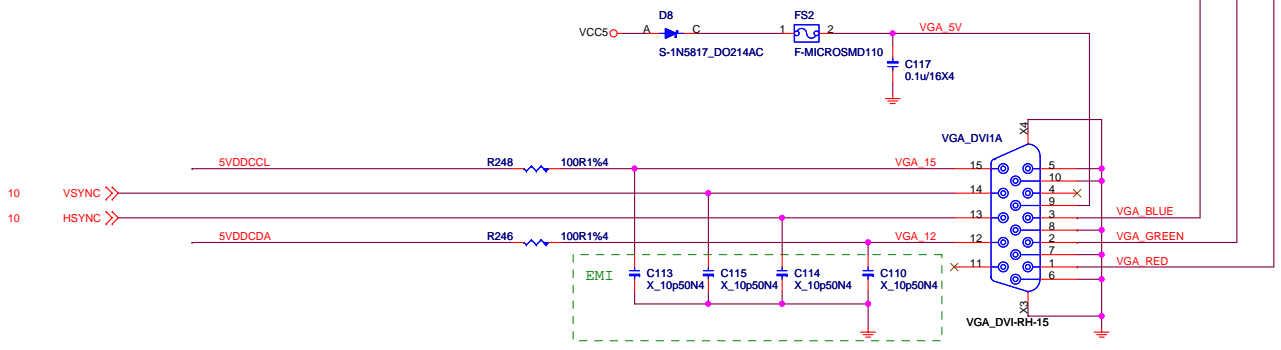
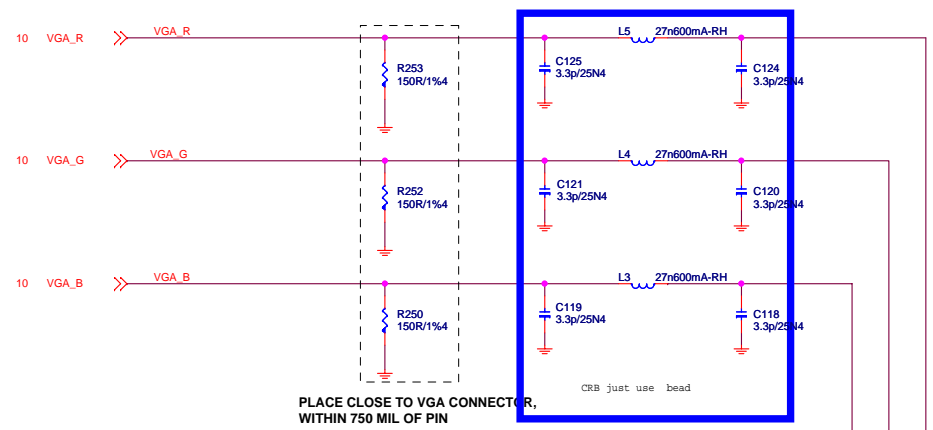
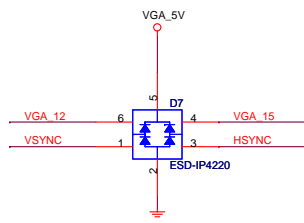
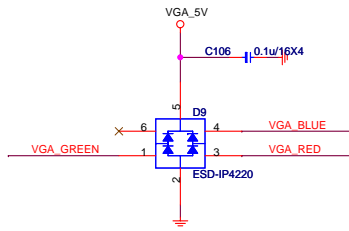
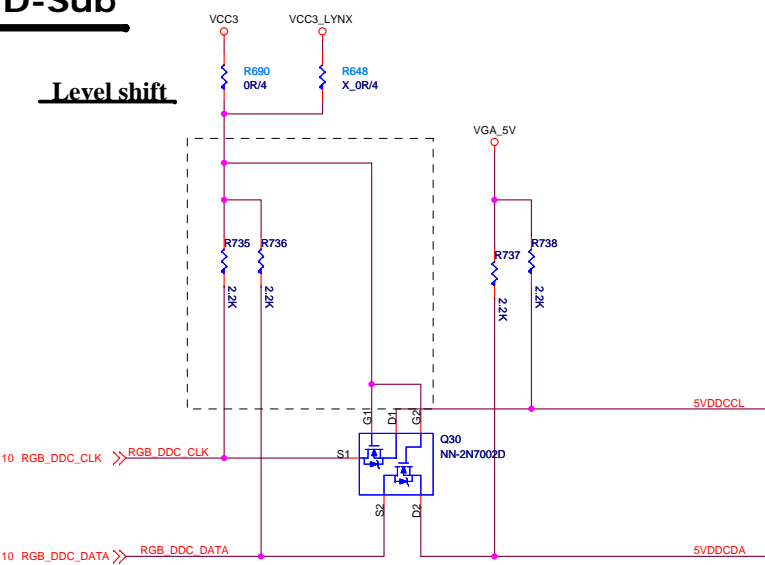


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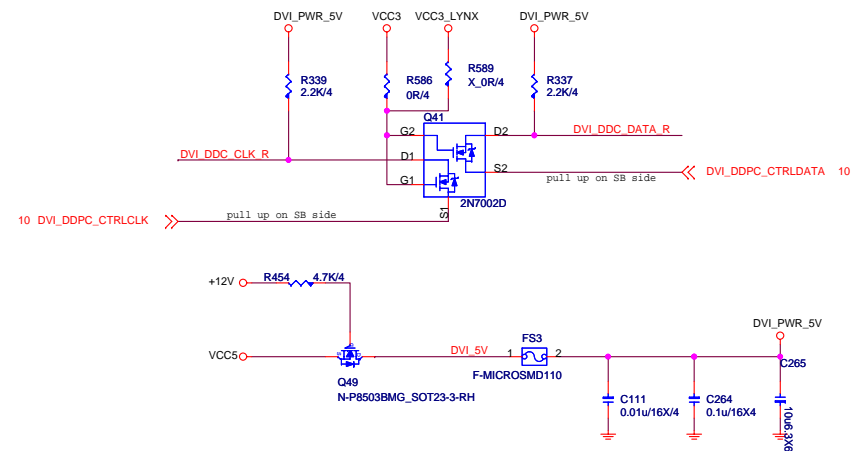
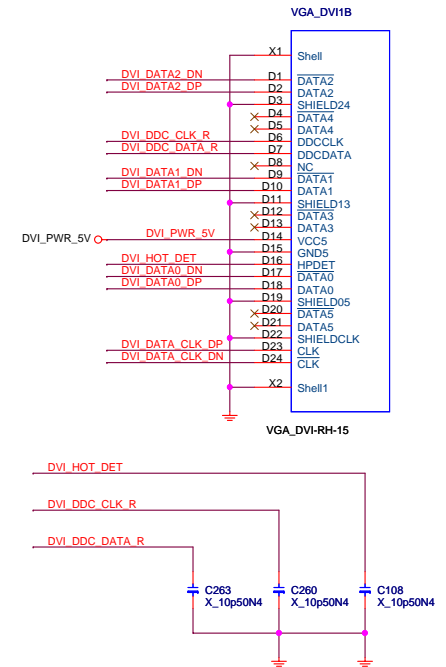
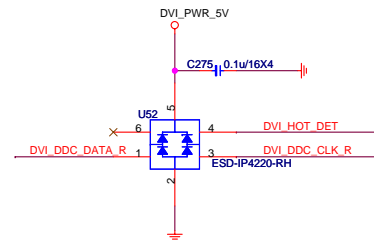
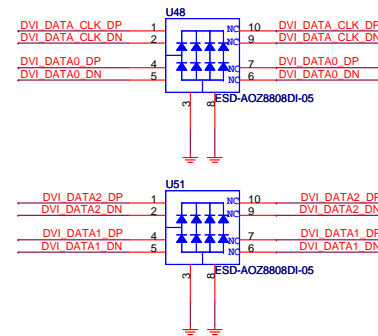
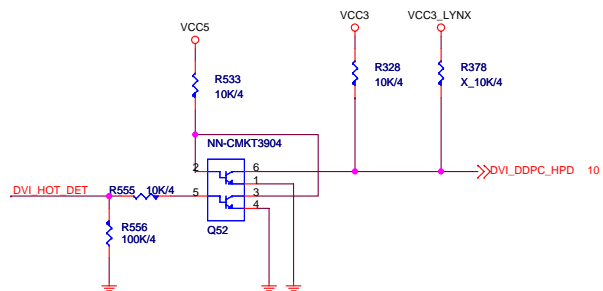
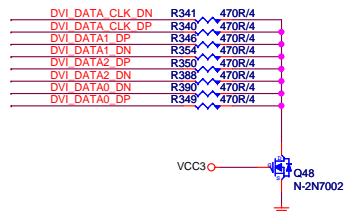
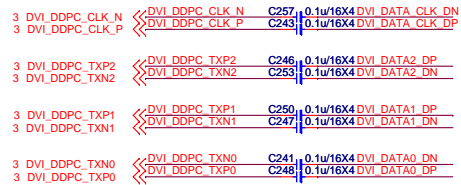
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D-Sub

LevelShift



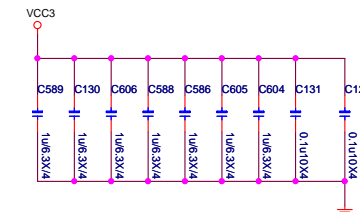
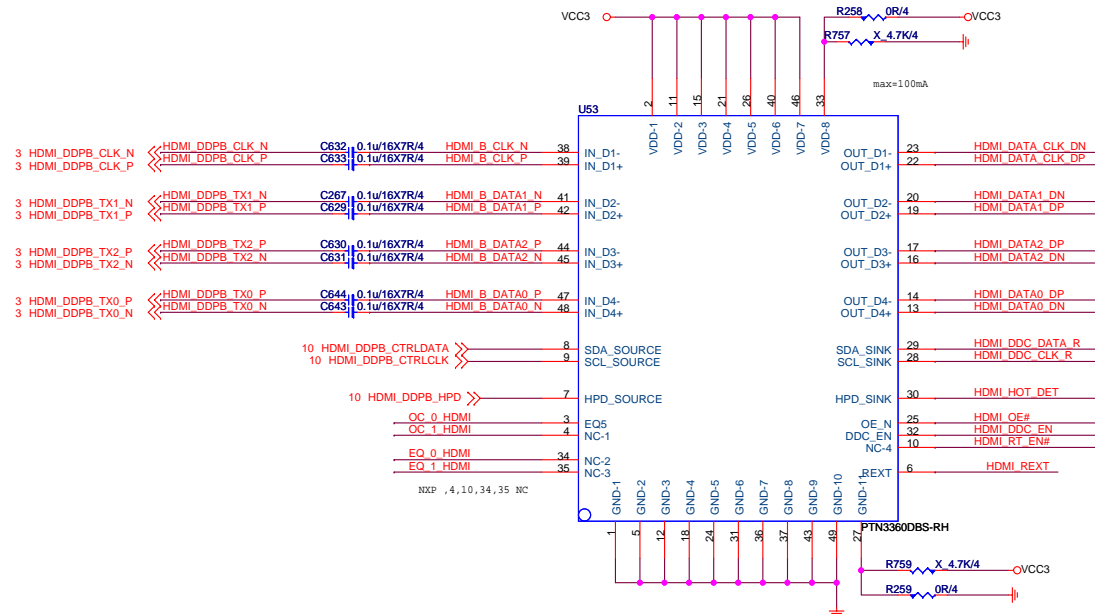
DVI level shifter



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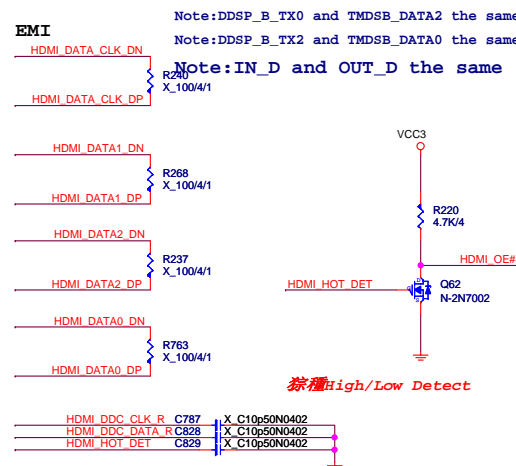
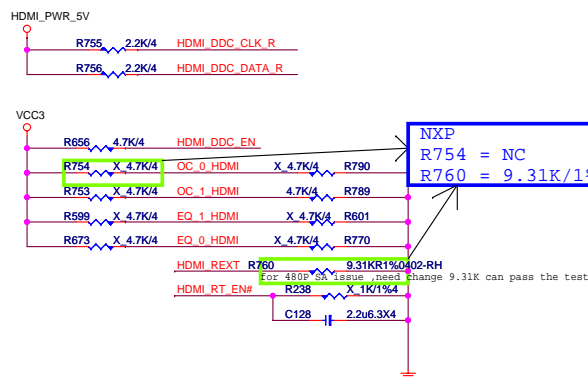
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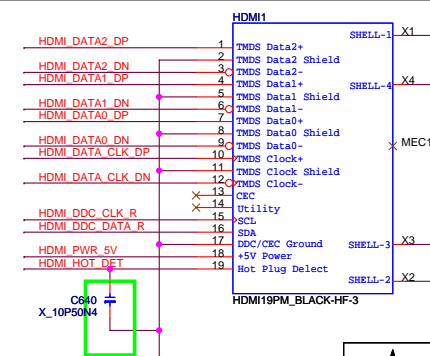
	"0"	"1"	note
HDMI_DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		5V tolerant, internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	PC1, PC0	note
1, 0, X	On	Off	00	8 dB
1, 1, 0	Off	On	01	4 dB
1, 1, 1	Off	Off	10	12 dB
0, X, X	Off	Off	11	0 dB



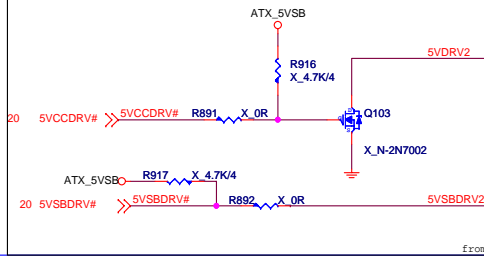
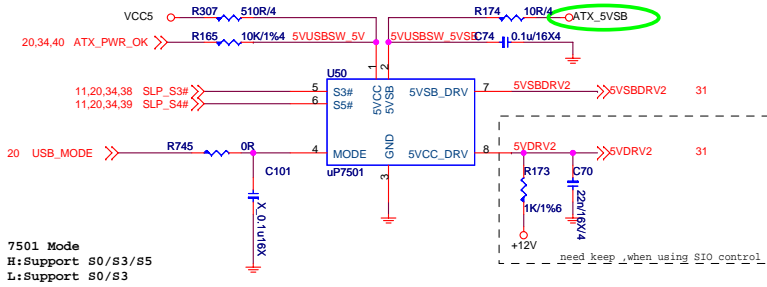
禁種High/Low Detect

Note: Reserve RN4; RN5 for EMI

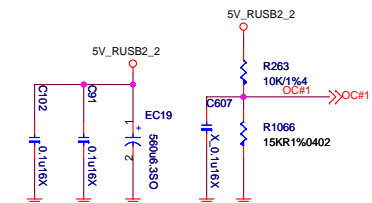
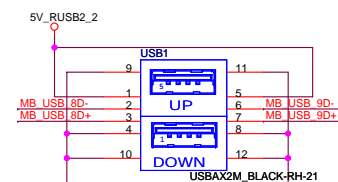
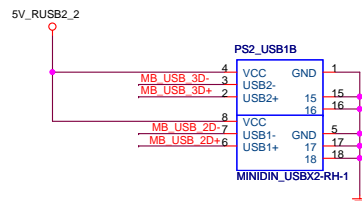
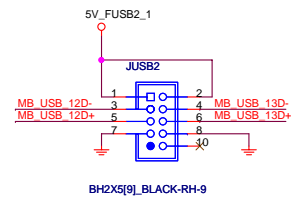
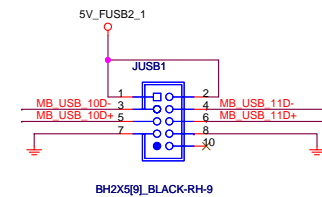
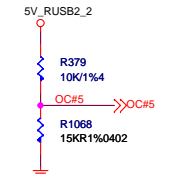
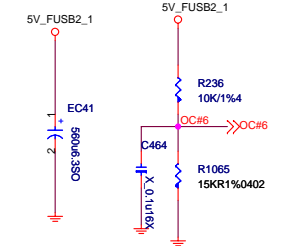
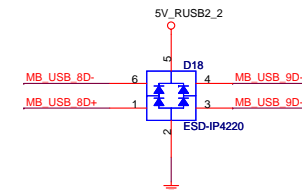
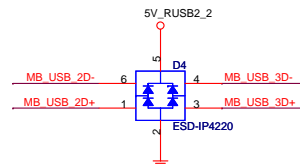
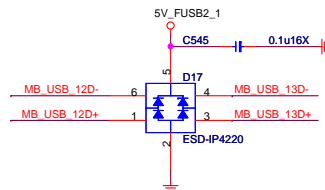
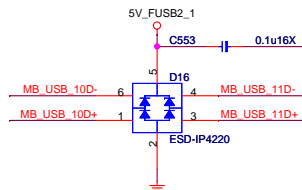
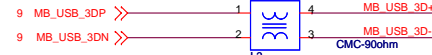
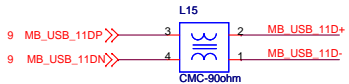
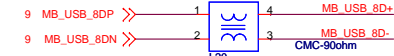
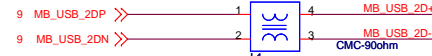
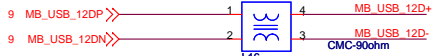
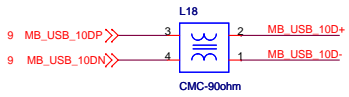
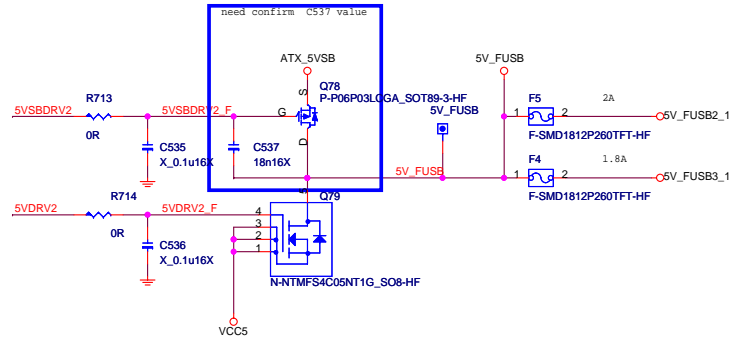
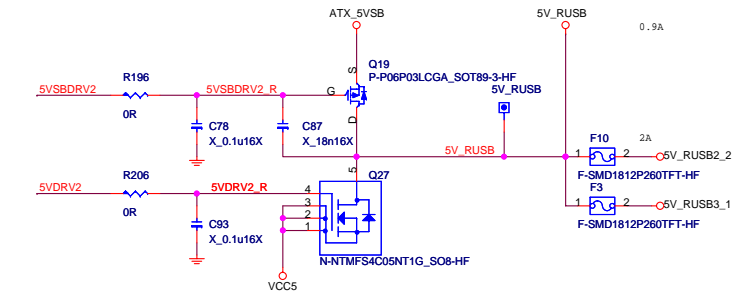
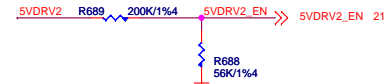


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5VDIMM FOR DDR



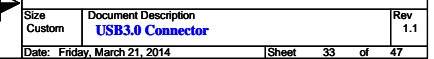
USB MODE

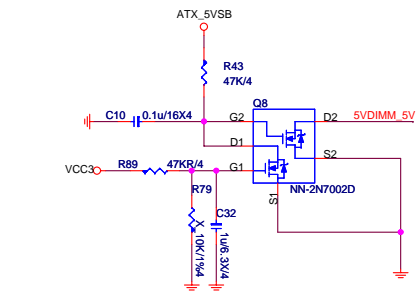


MICRO-STAR INT'L CO.,LTD

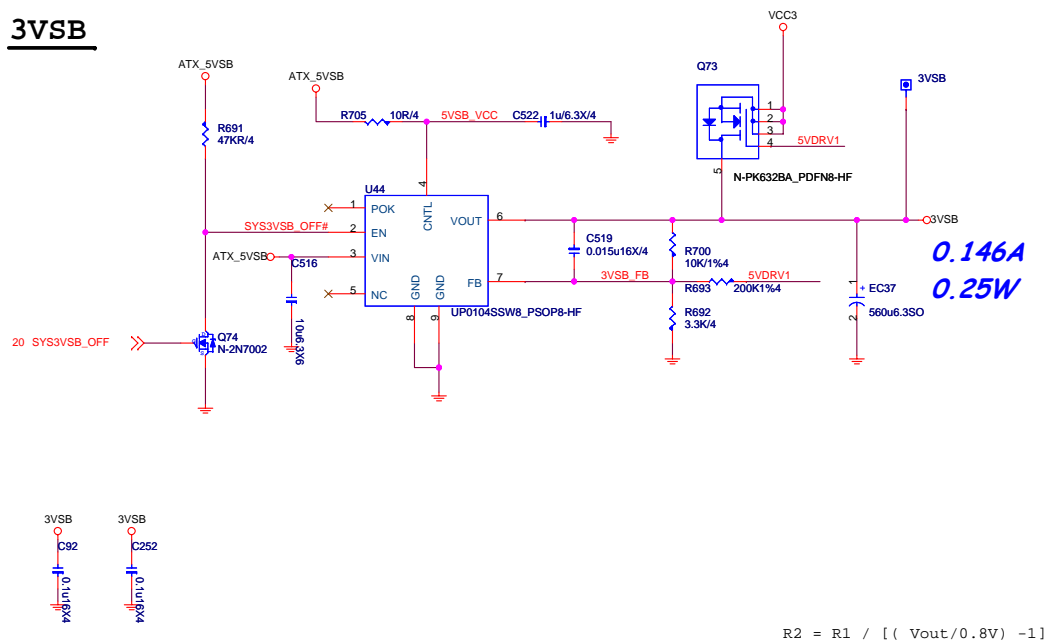
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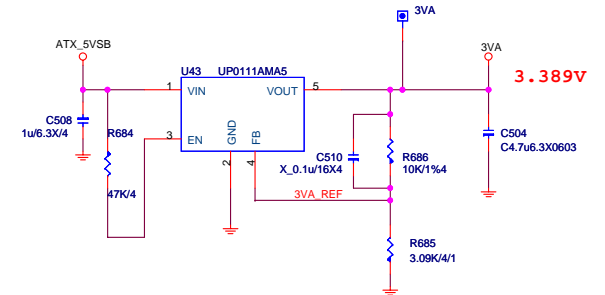




3VSB



3VA

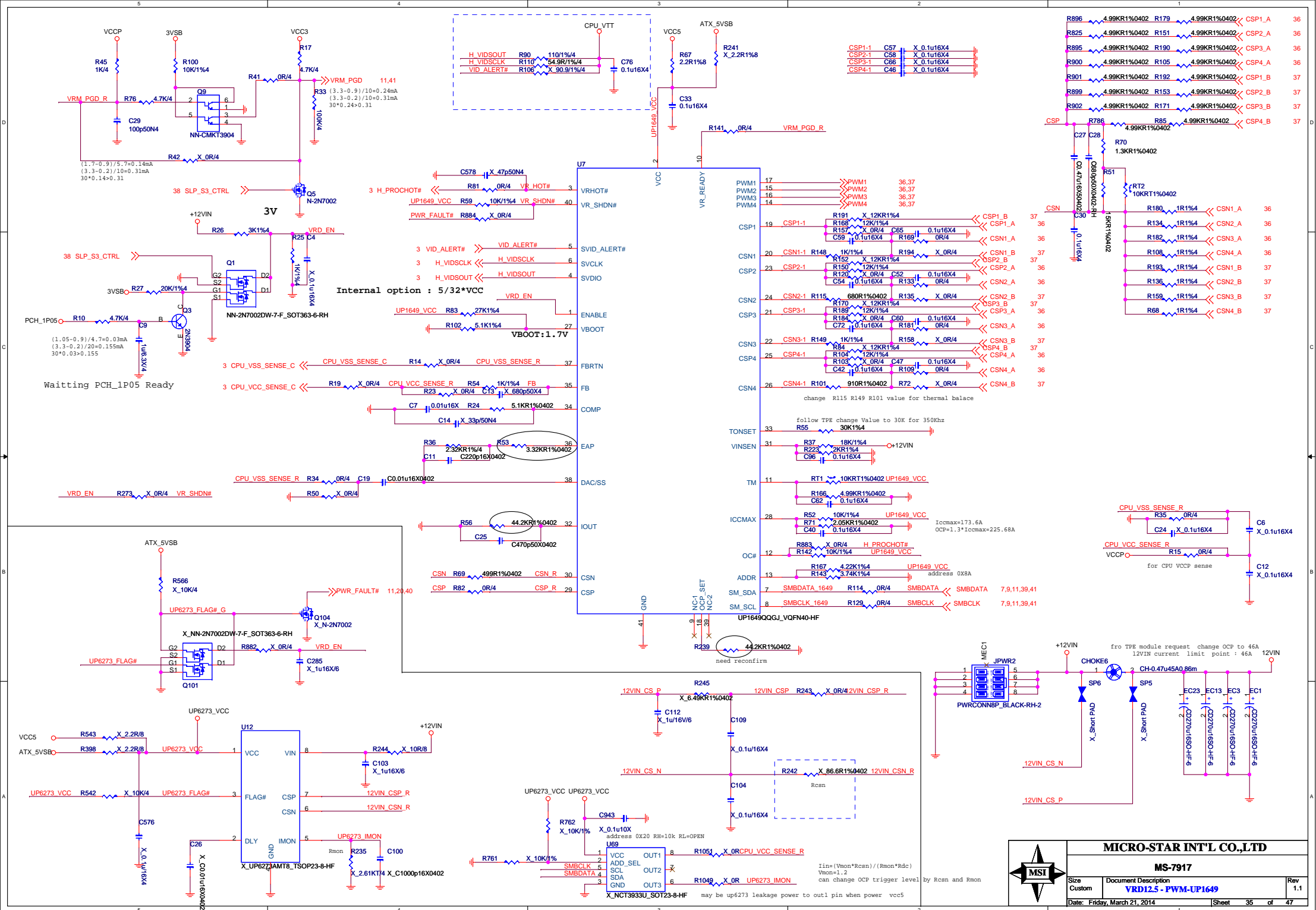


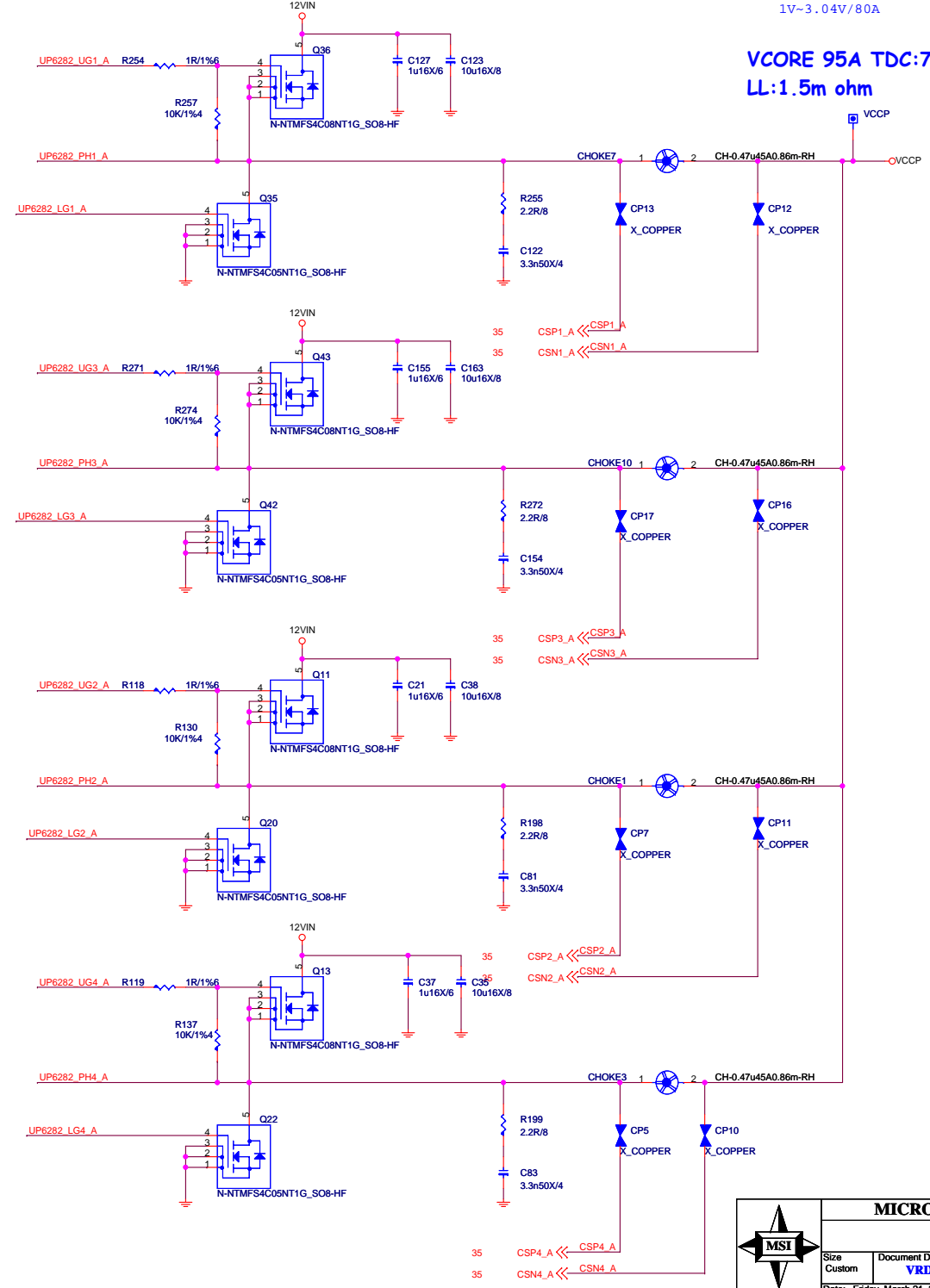
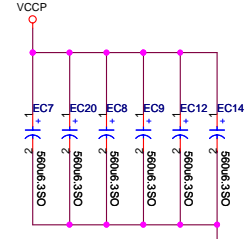
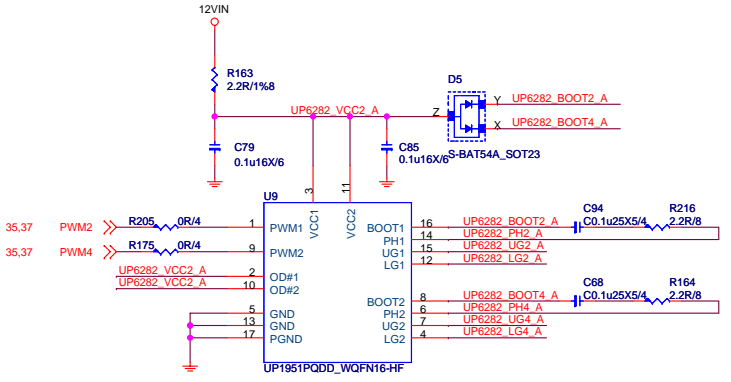
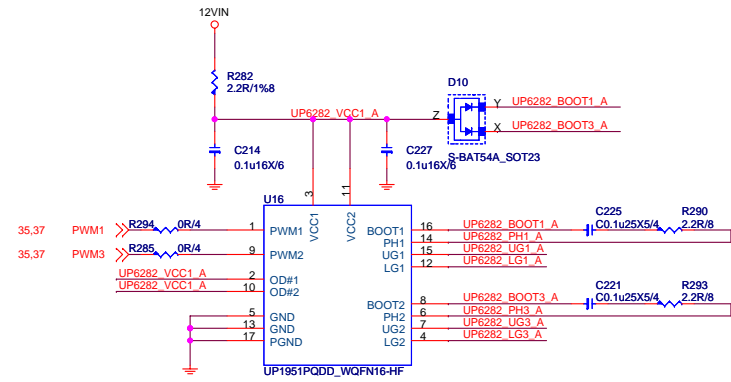
FOR DPWROK and 3VA sequence (S5-->G3->S5)



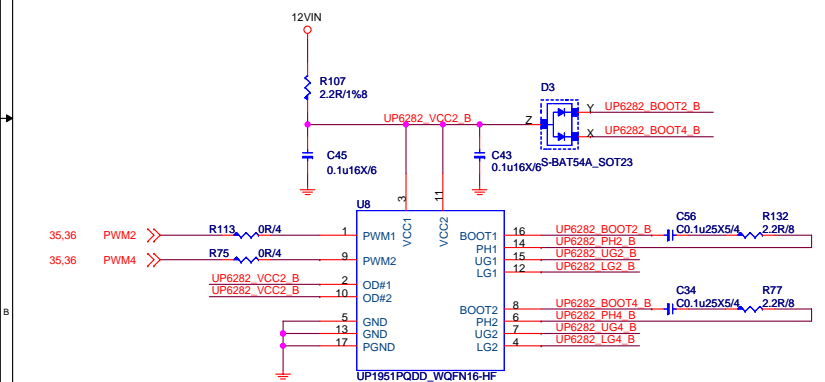
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1V~3.04V/80A
V CORE 95A TDC:70A
LL:1.5m ohm



VCORE 95A TDC:70A
LL:1.5m ohm

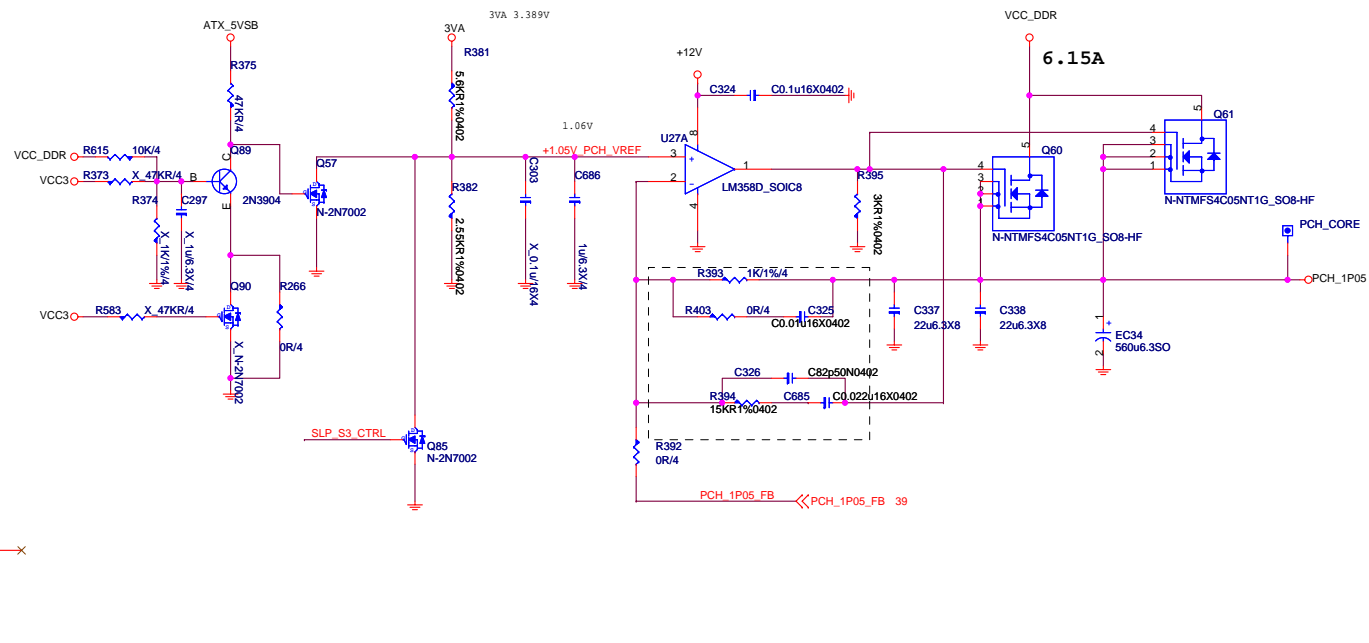


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1.05V_PCH

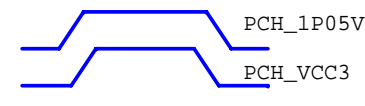


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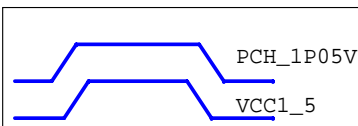
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

```

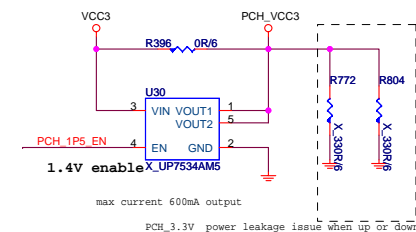
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VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



1.5VRUN

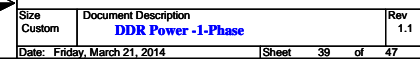


PCH Power:3.3V
0.188A

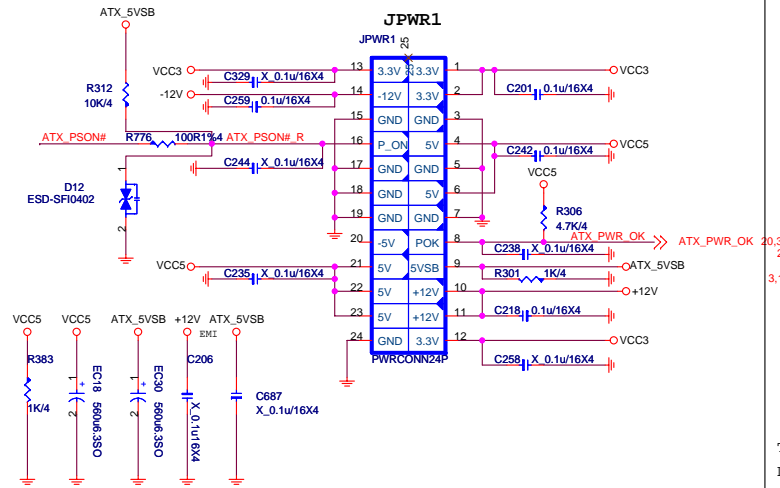


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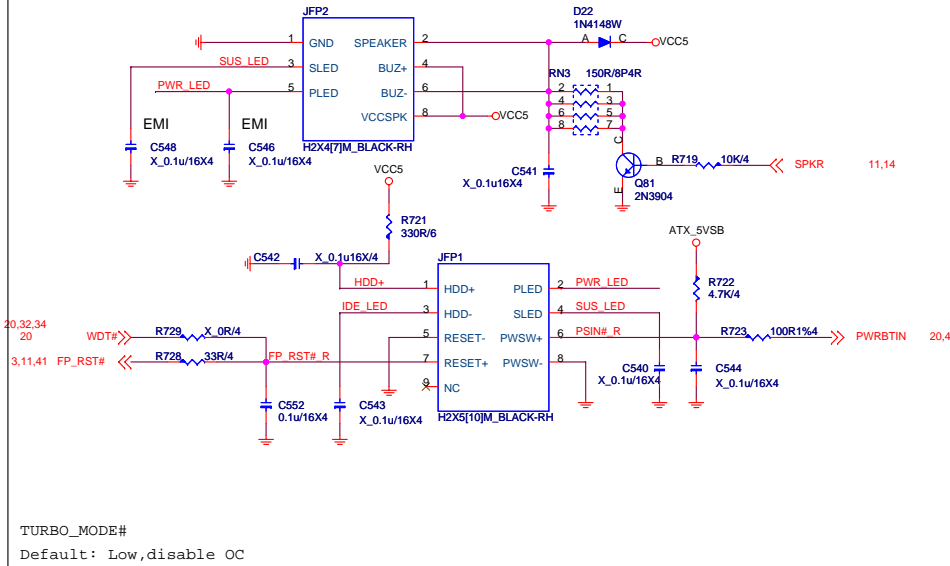
$OCP ((5*10v6*R758/(3.4/2))m\ ohm=36.47A>22.3*1.5A$



ATX POWER CONNECTOR

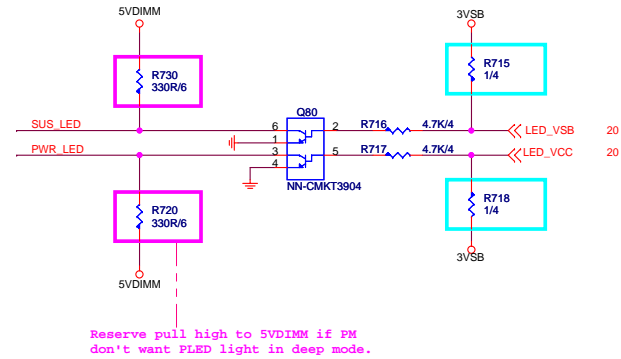


FRONT PANEL

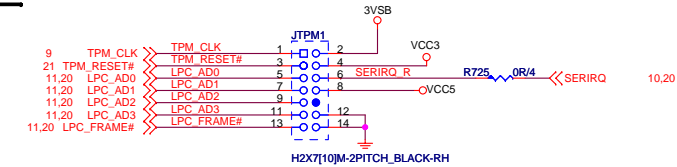


TURBO_MODE#
Default: Low,disable OC

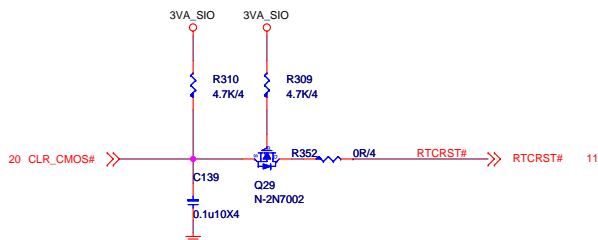
LED (for NCT6799D)



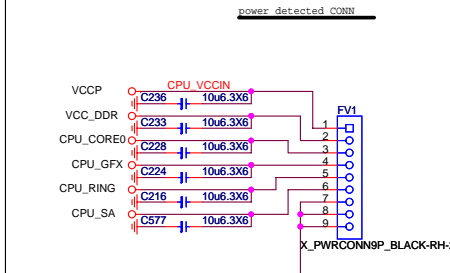
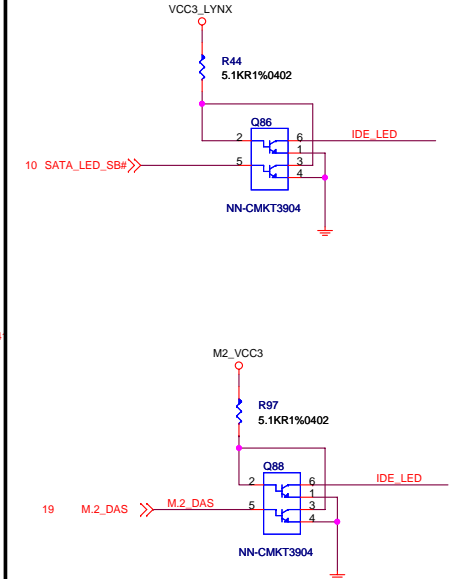
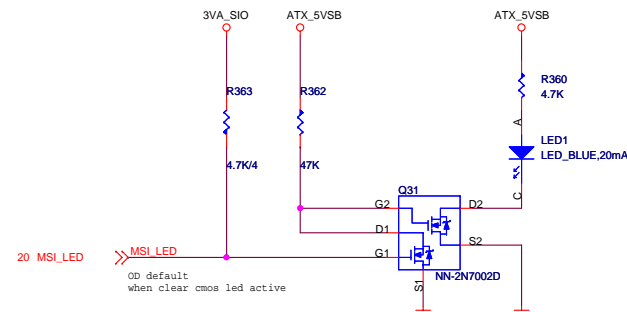
TPM



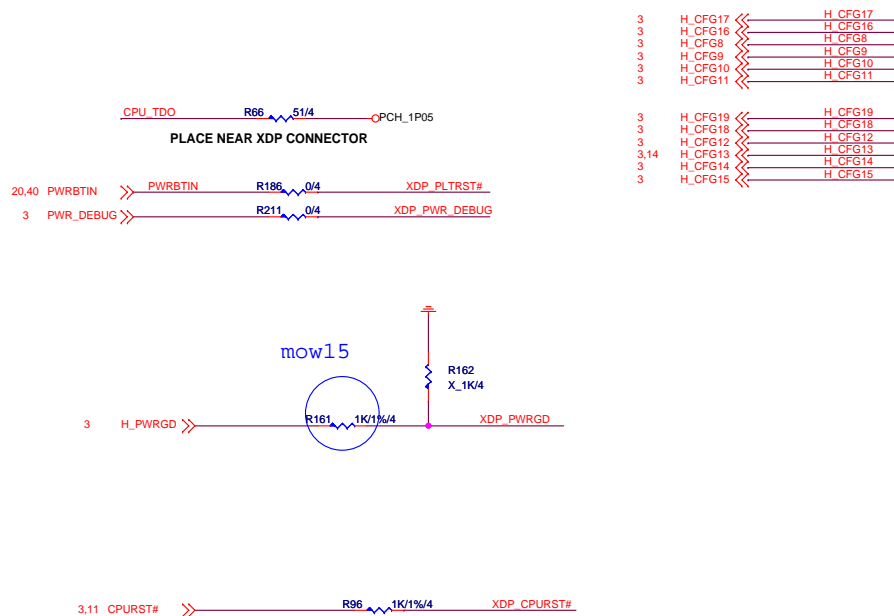
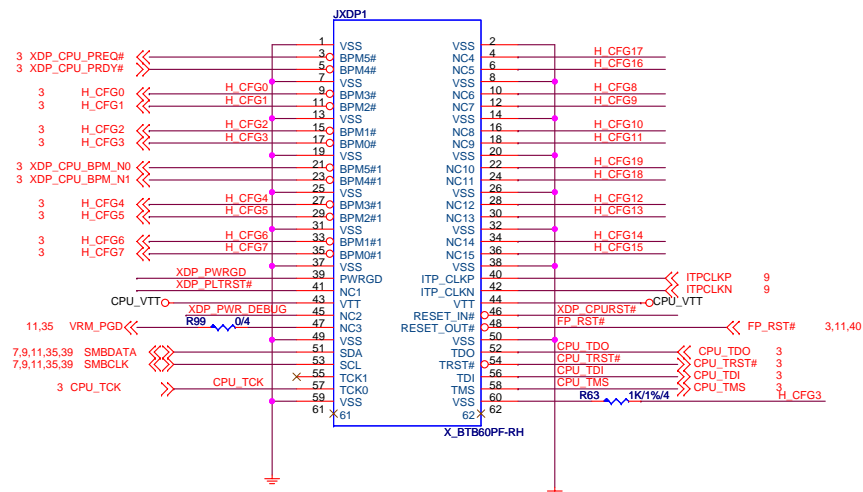
CLR+CMOS



MSI_LED



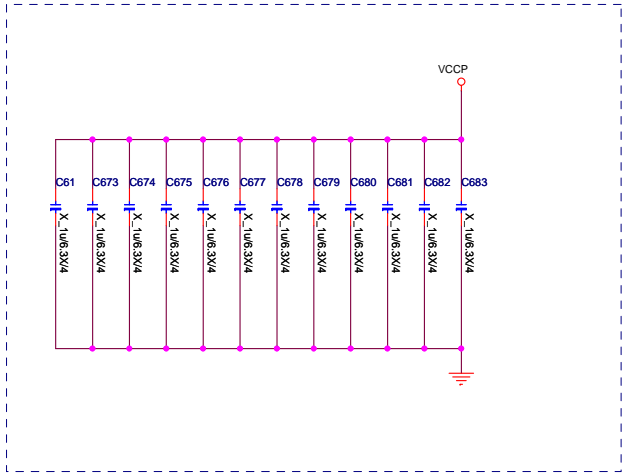
Reserve debug port 5020



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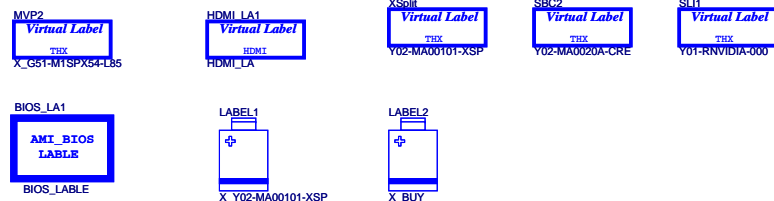
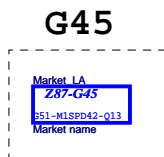
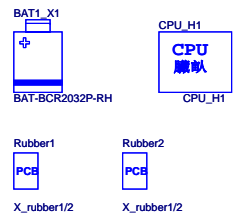
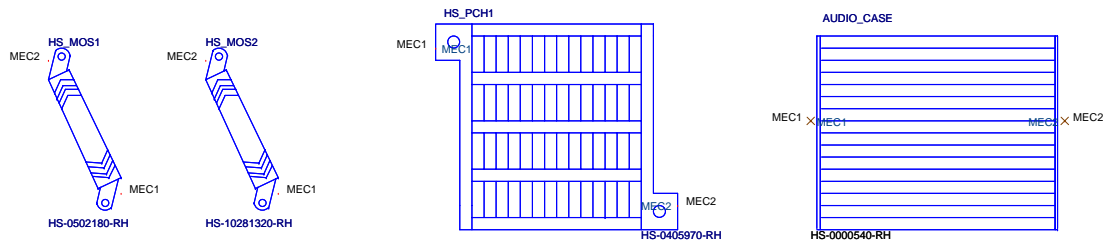
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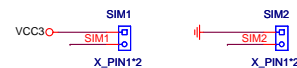
MICRO-STAR INT'L CO.,LTD

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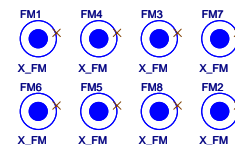
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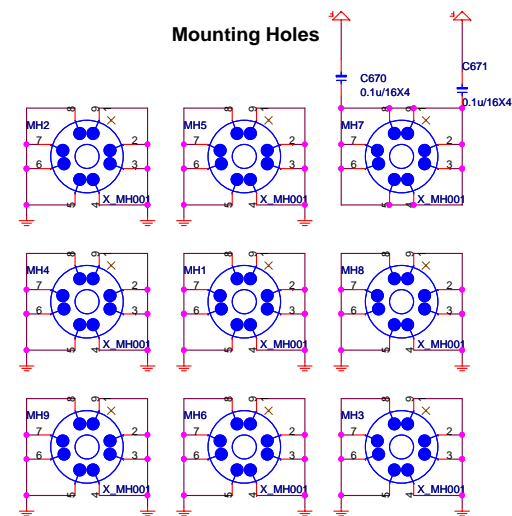
Simulation



Optical Fiducial Marks-120



Mounting Holes



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